SKP Engineering College

Tiruvannamalai – 606611

A Course Material

on

Electronic Circuits I

By

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Quality Certificate

This is to Certify that the Electronic Study Material

Subject Code: EC6301

Subject Name: Electronic Circuits I

Year/Sem: II/ III

Being prepared by me and it meets the knowledge requirement of the University curriculum.

Signature of the Author

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This is to certify that the course material being prepared by Mr. M.Jerin Jose is of the adequate quality. He has referred more than five books and one among them is from abroad author.

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EC6304 Electronic circuits I L T P C 3 0 0 3

Objective:

- To Learn about Biasing of BJTs and FETs.
- To Design and construct the Small Signal model of BJT Amplifiers.
- To Design and construct the Small Signal model of FET Amplifiers.
- To Study about the Frequency response of Amplifiers.
- To Design and Construct amplifiers with active loads

UNIT I BIASING OF DISCRETE BJT AND MOSFET 9

Rectifiers with Filters -DC Load line, operating point, various biasing methods for BJT Design-Stability-Bias compensation, Thermal stability, Design of biasing for JFET, Design of biasing for MOSFET.

UNIT II BJT AMPLIFIERS 9

Small signal Analysis of Common Emitter-AC Load line, Voltage swing limitations, Common collector and common base amplifiers – Differential amplifiers- CMRR-Darlington Amplifier- Bootstrap technique - Cascaded stages - Cascode Amplifier.Large signal Amplifiers-Class A, Class B and Class C power Amplifiers.

UNIT III JFET AND MOSFET AMPLIFIERS 9

Small signal analysis of JFET amplifiers- Small signal Analysis of MOSFET and JFET, Common source amplifier, Voltage swing limitations, Small signal analysis of MOSFET and JFET Source follower and Common Gate amplifiers, - BiMOS Cascode amplifier.

UNIT IV FREQUENCY ANALYSIS OF BJT AND MOSFET AMPLIFIERS 9

Low frequency and Miller effect, High frequency analysis of CE and MOSFET CS amplifier, Short circuit current gain, cut off frequency – fα and fβ unity gain and Determination of bandwidth of single stage and multistage amplifiers.

UNIT V IC MOSFET AMPLIFIERS 9

IC Amplifiers- IC biasing Current steering circuit using MOSFET- MOSFET current sources- PMOS and NMOS current sources. Amplifier with active loads - enhancement load, Depletion load and PMOS and NMOS current sources load- CMOS common source and source follower- CMOS differential amplifier-CMRR.

OUTCOMES:

Upon Completion of the course, the students will be able to:

- design various biasing circuits for all the type of transistors to keep the operating point Stable.
- design and analyze the small signal equivalent circuits of BJT Amplifiers
- design and analyze the small signal equivalent circuits of FET Amplifiers
- design and analyze the Frequency Response of Amplifiers

- design and analyze the different types of current mirror used for biasing.

TEXT BOOK

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CONTENTS

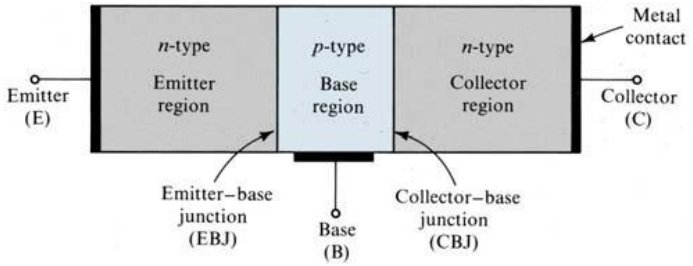
Unit- I

Biasing Of Discrete BJT and MOSFET

Part- A

1. Describe about BJT? [CO1-L1]

BJT consists of 2 PN junctions. It has three terminals: emitter, base and collector. Transistor can be operated in three regions, namely cut-off, active and saturation by applying proper biasing conditions.



2. List the operating regions of the transistor [CO1-L2]

Active:

– Most important mode, e.g. for amplifier operation and switching application
– The region where current curves are practically flat.

Saturation:

– Barrier potential of the junctions cancels each other out causing a virtual short.
– Ideal transistor behaves like a closed switch.

Cutoff:

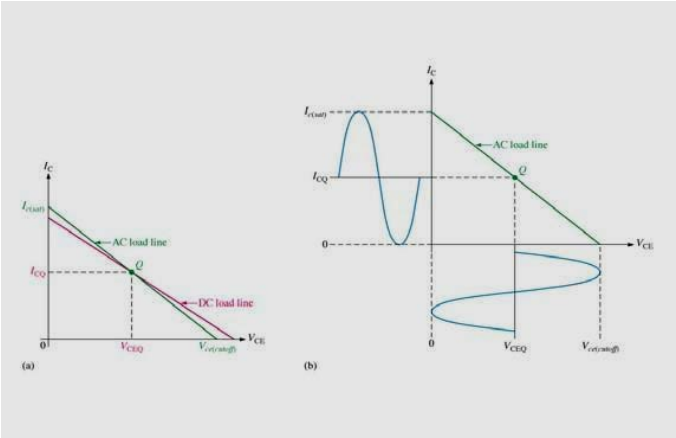
– Current reduced to zero
– Ideal transistor behaves like an open switch.

3. What is need of biasing? [CO1-L1]

Bias establishes the DC operating point for proper linear operation of an amplifier. If an amplifier is not biased with correct DC voltages on the input and output, it can go into saturation or cutoff when an input signal is applied.

4. Why do we choose Q point at the center of the load line? [CO1-L13

The output signal is sinusoidal waveform without any distortion. Thus point Q is the best operating point.



5. Name the two techniques used in the stability of the q point. [**CO1-L2]**

Stabilization technique:

It refers to the use of resistive biasing circuits which allow I_B to vary so as to keep I_C relatively constant with variations in I_{CO}, β and V_{BE}.

Compensation technique:

It refers to the use of temperature sensitive devices such as diodes, transistors, thermistors which provide compensating voltage and current to maintain Q point stable.

6. Give the expression for stability factor? [**CO1-L3]**

It is defined as the degree of change in operating point due to variation in temperature. There are three variables which are temperature dependent. Three stability factors are defined as follows,

i) $S = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\,\beta \text{ constant}}$ or $S = \left.\frac{\Delta I_C}{\Delta I_{CO}}\right|_{V_{BE},\beta \text{ constant}}$

ii) $S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\,\beta \text{ constant}}$ or $S' = \left.\frac{\Delta I_C}{\Delta V_{BE}}\right|_{I_{CO},\,\beta \text{ constant}}$

iii) $S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},\,V_{BE} \text{ constant}}$ or $S'' = \left.\frac{\Delta I_C}{\Delta \beta}\right|_{I_{CO},\,V_{BE} \text{ constant}}$

7. **What is meant by FET biasing**? [**CO1-L1]**

- The Parameters of FET is temperature dependent .When temperature increases drain resistance also increases, thus reducing the drain current.
- Unlike BJTs, thermal runaway does not occur with FET
- However, the wide differences in maximum and minimum transfer characteristics make I_D levels unpredictable with simple fixed-gate bias

voltage.

8. What are the different biasing circuits? [**CO1-L1]**

- Fixed bias circuits
- Self bias circuits
- Voltage bias circuits

9. What are the requirements of a biasing circuit? [**CO1-L2]**

a. Emitter base junction must be forward biased and collector base junction must be reverse biased. That means the transistor should be operated in the middle of the active region or Q point should be fixed at the centre of the active region.
b. Circuit design should provide a degree of temperature stability.
c. Q point should be made independent of the transistor parameters such as β.

10. Merits of stability factor? [**CO1-L2]**

- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (R_B).

- A very small number of components are required.

11 Define operating point. ***(May,15)*** [**CO1-L1]**

The zero signal values of Ic & Vce are known as operating point. It is also called so because the variations of Ic and Vce take place about this point, when the signal is applied.

12 Why the operating point is selected at the centre of the active region? [**CO1-L1]**

The operating point of a transistor is kept fixed usually at the center of the active region in order that the input signal is well amplified. If the point is fixed in the saturation region or the cut off region the positive and negative half cycle gets clipped off respectively.

13 What is DC load line? [**CO1-L1]**

It is the line on the output characteristics of a transistor circuit which gives the values of Ic & Vce corresponding to zero signal (or) DC Conditions.

14 What is the need for biasing in transistor amplifier? [**CO1-L1]**

The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is known as transistor biasing.

When a transistor is biased properly, it works efficiently and produces no distortion in the output signal and thus operating point can be maintained stable.

15. What are the factors to be considered to design a biasing circuit? *(May,15)* [**CO1**-**L1]**

It should ensure proper zero signal collector current.

The emitter base junction must be forward biased and collector base junction must be reversing biased.

The transistor should be operated in the middle of the active region or operation point should be fixed at the centre of the active region.

The operating point should be made independent of the transistor parameters (such as β). It should ensure that *VCE* does not fall below 0.5 V for *Ge* transistors and 1 V for

silicon transistors at any instant.

16. List out different type of biasing. [**CO1**-**L1]**

i. Voltage divider bias
ii. Fixed bias
iii. Emitter feedback bias
iv. Collector feedback bias

17. Define stability factor of an amplifier. What is ideal value? [**CO1**-**L2]**

*The rate of change of collector current IC w.r.t. the collector leakage current *ICO at constant* β *and IB is called* **stability factor** *i.e.*

Stability factor, $S = dI_C / Ico\ dI$ *at constant* I_B *and* β

18. What is thermal run away in a transistor? *(Nov/Dec 2006) (Nov/Dec 2008)* [**CO1**-**L1]**

The collector current, being equal increases with increase in temperature .This leads to increased power dissipation with further increase in temperature. .Being accumulative process it can lead to thermal runaway resulting in burn out of transistor. Self destruction of an un-stabilized transistor is called thermal runaway.

19. **Why thermal runaway is not there in FETs?** [**CO1**-**L2]**

The FET has a positive temperature coefficient of resistivity. In FET, as temperature increases its drain resistance also increases, reducing the drain current. Thus, unlike BJT, thermal runaway does not occur with FET.

20. What are the advantages and disadvantages of fixed bias circuits? [**CO1**-**L1]**

Merits:

- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (R_B).

- A very small number of components are required.

Demerits:

- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- Changes in V_{be} will change I_B and thus cause R_E to change. This in turn will alter the gain of the stage.

- When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.

- For small-signal transistors (e.g., not power transistors) with relatively high values of β (i.e., between 100 and 200), this configuration will be prone to thermal runaway. In particular, the stability factor, which is a measure of the change in collector current with changes in reverse saturation current, is approximately β+1. To ensure absolute stability of the amplifier, a stability factor of less than 25 is preferred, and so small-signal transistors have large stability factors.

21.How self-bias circuit is used as constant current source? [**CO1**-**L1]**

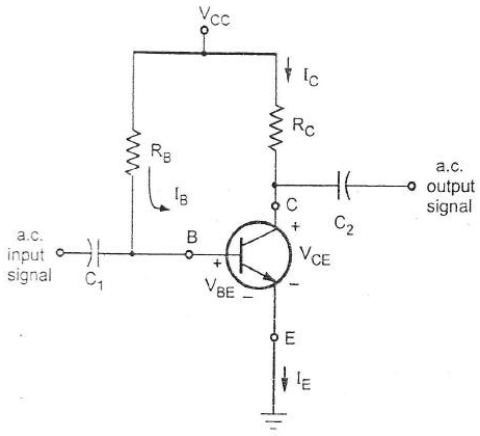
In the self bias circuit if Ic tends to increase because of ICO has increasing as a result of temperature, the current in RE increases. As consequences of the increase in voltage drop across RE that provides negative feedback, the base current is decreased. Hence constant IC value is maintained in the self bias circuit.

22. **How FET is known as Voltage variable resistor?** [**CO1**-**L2]**

In the region before pinch off, where VDS is small, the drain to source resistance rd can be controlled by the bias voltage VGS. Therefore FET is useful as voltage variable resistor (VVR) or Voltage dependent Resistor (VDR)

PART-B

1. Explain the fixed bias method & derive an expression for stability factors. [CO1-H1]



The Figure shows the fixed bias circuit. It is the simplest d.c. bias configuration. For the d.c. analysis we can replace capacitor with an open circuit because the reactance of a capacitor for dc. is

$$X_C = 1 / 2\pi fC = 1 / 2\pi(0)C = \infty.$$

In the base circuit, Apply KVL, we get

$$VCC = IBRB + VBE$$

Therefore,

$$I_B = (V_{CC} - V_{BE})/R_B$$

For a given transistor, V_{BE} does not vary significantly during use. As V_{CC} is of fixed value, on selection of R_B, the base current I_B is fixed. Therefore this type is called *fixed bias* type of circuit.

In the Collector circuit

Apply KVL, we get

$$V_{CC} = I_C R_C + V_{CE}$$

Therefore,

$$VCE = VCC - ICRC$$

The common-emitter current gain of a transistor is an important parameter in circuit design, and is specified on the data sheet for a particular transistor. It is denoted as β.

$$I_C = \beta I_B$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$V_{CE} = V_C - V_E$$

$$V_{BE} = V_B - V_E$$

In this circuit $V_E = 0$

$$V_{BE} = V_B$$

$$V_{CE} = V_C$$

Stability factor S for Fixed bias circuit

Stability Factor S

$$I_B \cong \frac{V_{CC}}{R_B}$$

When I_B changes by ∂I_B, V_{CC} and V_{BE} are unaffected.

$\therefore \frac{\partial I_B}{\partial I_C} = 0$ $\because I_C$ is not present in the equation.

Substituting this value in equation , we get,

$$S = \frac{1+\beta}{1-\beta(\partial I_B / \partial I_C)} = \frac{1+\beta}{1-0}$$

$$\therefore \quad S = 1 + \beta$$

Merits:

- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (R_B).
- A very small number of components are required.

Demerits:

- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- Changes in V_{be} will change I_B and thus cause R_E to change. This in turn will alter the gain of the stage.
- When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.
- For small-signal transistors (e.g., not power transistors) with relatively high values of β (i.e., between 100 and 200),

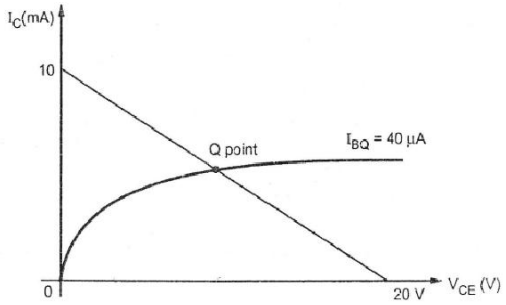
This configuration will be prone to thermal runaway. In particular, the stability factor,

which is a measure of the change in collector current with changes in reverse saturation current, is approximately β+1. To ensure absolute stability of the amplifier, a stability factor of less than 25 is preferred, and so small signal transistors have large stability factors.

Usage:

Due to the above inherent drawbacks, fixed bias is rarely used in linear circuits (i.e., those circuits which use the transistor as a current source). Instead, it is often used in circuits where transistor is used as a switch. However, one application of fixed bias is to achieve crude automatic gain control in the transistor by feeding the base resistor from a DC signal derived from the AC output of a later stage.

2. Design the fixed bias circuit from the load line given in the figure. [CO1-H2]



Solution : From the load line we have,

$$V_{CC} = 20 \text{ V}$$

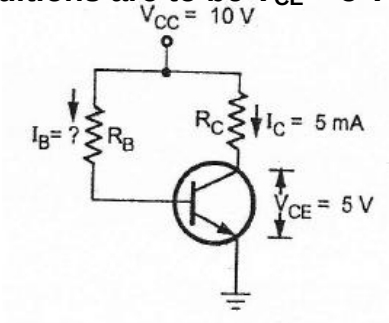
$$\frac{V_{CC}}{R_C} = 10 \times 10^{-3} \qquad \therefore \quad R_C = \frac{20}{10 \times 10^{-3}} = 2 \text{ K}$$

We have, $$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 - 0.7 \text{ V}}{40 \times 10^{-6}}$$

$$= 482.5 \text{ k}\Omega$$

3. Design a fixed biased circuit using a silicon transistor having β value of 100. Vcc is 10 V and dc bias conditions are to be V_{CE} = 5 V and I_C = 5 mA, [CO1-H3]



Solution

Applying KVL to collector circuit,

$$V_{CC} - V_{CE} - I_C R_C = 0$$

$$\therefore R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{10 - 5}{5\,mA} = 1\ K$$

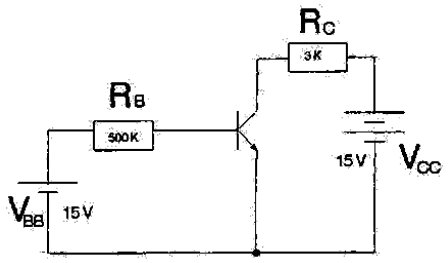
$$I_B = \frac{I_C}{\beta} = \frac{5\,mA}{100} = 50\ \mu A$$

Applying KVL to base circuit,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{10 - 0.7}{50\,\mu A} = 186\ k\Omega$$

4. Calculate the operating point (Q-point)? [CO1-H1]



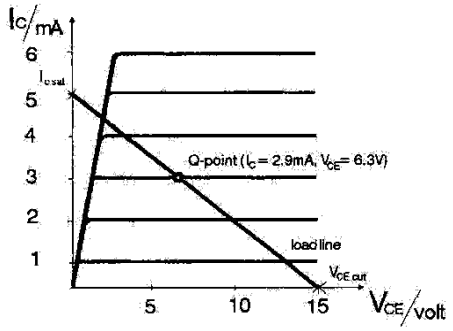
Base biased CE connection

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{14.3V}{500K\Omega} = 29\mu A$$

$I_C = \beta_{dc} * I_B = 100 * 29\mu A = 2.9$ mA

$V_{CE} = V_{CC} - (I_C * R_C) = 15V - (2.9\ mA * 3K\Omega) = 6.3V$

By plotting I_C (2.9 mA) and V_{CE} (6.3V), we get the operation point ----> Q-point (quieSKPnt point).



Collector curve with load line and Q – point

5. What are the Method of stabilizing the Q point [CO1-H1]

Stabilization technique:

It refers to the use of resistive biasing circuits which allow I_B to vary so as to keep I_C relatively constant with variations in I_{CO}, β and V_{BE}.

Compensation technique:

It refers to the use of temperature sensitive devices such as diodes, transistors, thermistors which provide compensating voltage and current to maintain Q point stable.

Stability Factors

It is defined as the degree of change in operating point due to variation in temperature. There are three variables which are temperature dependent. Three stability factors are defined as follows,

i) $$S = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\,\beta \text{ constant}} \quad \text{or} \quad S = \left.\frac{\Delta I_C}{\Delta I_{CO}}\right|_{V_{BE},\,\beta \text{ constant}}$$

ii) $$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\,\beta \text{ constant}} \quad \text{or} \quad S' = \left.\frac{\Delta I_C}{\Delta V_{BE}}\right|_{I_{CO},\,\beta \text{ constant}}$$

iii) $$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},\,V_{BE} \text{ constant}} \quad \text{or} \quad S'' = \left.\frac{\Delta I_C}{\Delta \beta}\right|_{I_{CO},\,V_{BE} \text{ constant}}$$

Stability factor S:

For a common emitter configuration collector current is given as,

$$I_C = \beta I_B + I_{CEO}$$

or $$I_C = \beta I_B + (1+\beta) I_{CBO}$$

When I_{CBO} changes by ΔI_{CBO}, I_B changes by ∂I_B and I_C changes by ∂I_C. equation becomes,

$$\partial I_C = \beta \partial I_B + (1+\beta) \partial I_{CBO}$$

$$\therefore \quad 1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta) \frac{\partial I_{CBO}}{\partial I_C}$$

$$\therefore \quad 1 - \beta \frac{\partial I_B}{\partial I_C} = (1+\beta) \frac{\partial I_{CBO}}{\partial I_C}$$

$$\therefore \quad \frac{\partial I_{CBO}}{\partial I_C} = \frac{1 - \beta (\partial I_B / \partial I_C)}{1+\beta}$$

The above equation can be considered as a standard equation for the derivation of stability factors of other biasing circuits.

Stability factor S':

$$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\beta \text{ constant}}$$

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

Stability factor S":

$$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{V_{BE}, I_{CO}\ \text{constant}}$$

From equation (1.7.7) we have $I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (\beta + 1) I_{CBO}$

$$\therefore \quad \frac{\partial I_C}{\partial \beta} = \left(\frac{V_{CC}}{R_B} - \frac{V_{BE}}{R_B}\right) + I_{CBO} = I_B + I_{CBO} = \frac{I_C}{\beta}$$

$$\therefore \quad \frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta} \quad \text{Since } I_B = \frac{I_C}{\beta} \text{ and } I_B >> I_{CBO}$$

Relation between S and S":

We know that S = 1+β and S" = I_C/β

Multiplying numerator and denominator by (1+β),

$$S'' = I_C(1+\beta)$$

$$\frac{\qquad}{\beta(1+\beta)}$$

$$S'' = I_C\ S$$

$$\frac{\qquad}{\beta(1+\beta)}$$

6. **Explain about Collector to Base Bias circuit [CO1-H2]**

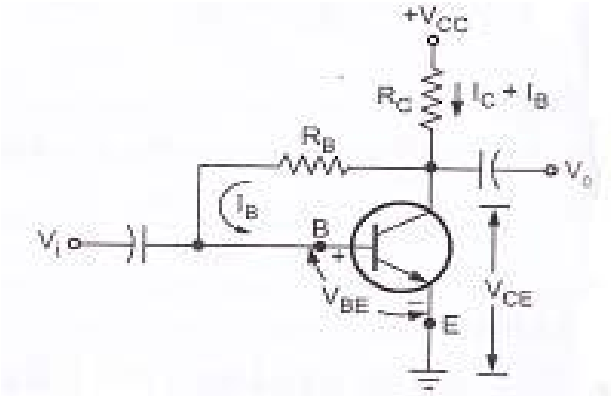


Fig. D.C. bias with voltage feedback

Figure shows the dc bias with voltage feedback. It is also called as collector to base bias circuit. It is an improvement over fixed bias method. In this, biasing resistor is connected between collector and base of the transistor to provide feedback path.

Circuit analysis: Base circuit:

Consider the base circuit and applying voltage law then we get,

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} = (R_B + R_C) I_B + I_C R_C + V_{BE}$$

$$= (R_B + R_C) I_B + \beta I_B R_C + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_C}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C} \qquad \because \beta >> 1$$

Only the difference between the equation for I_B and that obtained for fixed bias configuration is βR_C, so the feedback path results in a reflection of the resistance R_C to the input circuit.

Collector circuit:

Applying KVL to the collector circuit,

$V_{CC} – (I_C + I_B) R_C – V_{CE} =$

$0\ V_{CE} = V_{CC} – (I_C + I_B) R_C$

If there is a change in β due to piece to piece variation between transistors or if there is a change in β and I_{CO} due to the change in temperature. So collector current tends to increase. As a result, voltage drop across R_C increases. Due to reduction in V_{CE}, I_B reduces. The result is that the circuit tends to maintain a stable value of collector current, keeping the Q point fixed.

In this circuit, R_B appears directly across input and output. A part of output is feedback to the input. And increase in collector current decreases the base current. So negative feedback exists in the circuit. It is also called as voltage feedback bias circuit.

Unit- II

BJT Amplifiers

Part- A

1. What is an amplifier? [**CO2-L1]**

An amplifier is used to increase the signal level. It is used to get a larger signal output from a small signal input. Assume a sinusoidal signal at the input of the amplifier. At the output, signal must remain sinusoidal in waveform with frequency same as that of input. To make the transistor work as an amplifier, it is to be biased to operate in active region. It means base-emitter junction is forward biased and base-collector junction is reverse biased.

Let us consider the common emitter amplifier circuit using voltage divider bias.

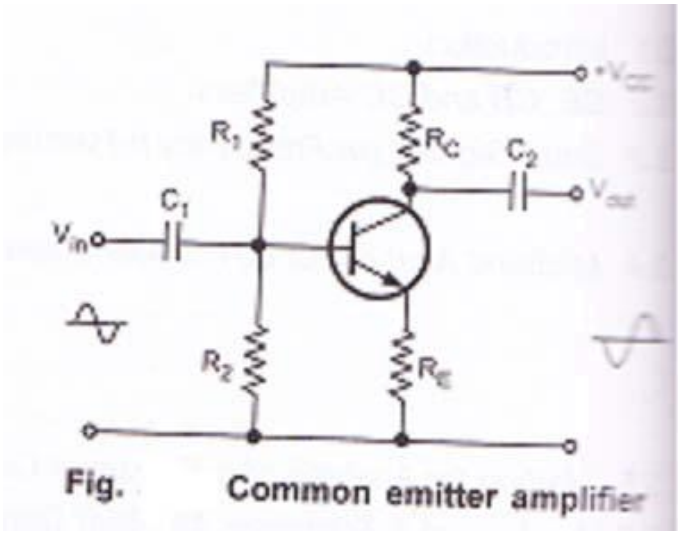


Fig. Common emitter amplifier

2. What are the main components present in the transistor circuits? [**CO2-L1]**

1. Biasing Circuit:

Resistors R_1, R_2 and R_E form the voltage divider biasing circuit for CE amplifier and it sets the proper operating point for CE amplifier.

2. Input Capacitor C_1:

C_1 couples the signal to base of the transistor. It blocks any D.C. component present in the signal and passes only A.C. signal for amplification.

3. Emitter Bypass Capacitor C_E:

C_E is connected in parallel with emitter resistance R_E to provide a low reactance path to the amplified A.C. This will reduce the output voltage and reducing the gain value.

4. Output Coupling Capacitor C_2:

C_2 couples the output of the amplifier to the load or to the next stage of the amplifier. It blocks D.C. and passes only A.C. part of the amplified signal.

3. what is mean by Phase reversal? [**CO2-L1]**

The phase relationship between the input and output voltages can be determined by considering the effect of positive and negative half cycle separately. The collector current is β times the base current, so the collector current will also increases. This increases the voltage drop across R_C.

$$V_C = V_{CC} - I_C R_C$$

4. What are the Benefits of h-parameters? [**CO2-L1]**

- Real numbers at audio frequencies
- Easy to measure
- Can be obtained from the transistor static characteristic curve
- Convenient to use in circuit analysis and design
- Most of the transistor manufacturers specify the h-parameters

5. What are the methods to analyze the transistor circuit? [**CO2-L2]**

The analysis of transistor circuits for small signal behaviour can be made by following simple guidelines. These guidelines are,

- Draw the actual circuit diagram
- Replace coupling capacitors and emitter bypass capacitor by short circuit
- Replace D.C. source by a short circuit
- Mark the points B, E, C on the circuit diagram and locate these points as the start of the equivalent circuit
- Replace the transistor by its h-parameter model

6. What are the two operating modes in the electronic circuits? [**CO2-L2]**

- Differential mode operation
- Common mode operation

7. List the types of amplifier configurations? [**CO2-L3]**

- Dual input balanced output differential amplifier.
- Dual input, unbalanced output differential amplifier.
- Single input, balanced output differential amplifier.
- Single input, unbalanced output differential amplifier.

8. How the impedance can be improved in the amplifiers? [**CO2-L1]**

The input impedance can be increased using two techniques :

- Using direct coupling (Darlington connection)
- Using Bootstrap technique

9. What is the coupling schemes used in multistage amplifiers? [**CO2-L2]**

we need amplifier which can amplify a signal from a very weak source such as a microphone, to a level which is suitable for the operation of another transducer such as loudspeaker . This is achieved by cascading number of amplifier stages, known as multistage amplifier

10. Define Common Mode Rejection Ratio (CMRR) [**CO2-L2**]

When the same voltage is applied to both the inputs, the differential amplifier is said to be operated in a common mode configuration. Many disturbance signals, noise signal appear as a common input signal to both the input terminals of the differential amplifier. Such a common signal should be rejected by the differential amplifier. The ability of a differential amplifier to reject a common mode signal is expressed by a ratio called common mode rejection ratio denoted as CMRR. It is defined as the ratio of the differential voltage gain A_d to common mode voltage gain A_C

$$\text{CMRR} = \rho = \left|\frac{A_d}{A_c}\right|$$

$$\text{CMRR in dB} = 20 \log \left|\frac{A_d}{A_c}\right| \text{dB}$$

11. Define voltage & current gain of an emitter follower. [**CO2-L1**]

The current gain of the emitter follower is nearly 20 to 500 times greater compared with other both configurations. Also the voltage is moderate.

12. What are the advantages of Representation of Gain in Decibels. [**CO2-L2**]

Logarithmic scale is preferred over linear scale to represent voltage and power gains because of the following reasons :

- In multistage amplifiers, it permits to add individual gains of the stages to calculate overall gain.
- It allows us to denote, both very small as well as very large quantities of linear, scale by considerably small figures.

For example, voltage gain of 0.0000001 can be represented as -140 dB and voltage gain of 1,00,000 can be represented as 100 dB.

- Many times output of the amplifier is fed to loudspeakers to produce sound which is received by the human ear. It is important to note that the ear responds to the sound intensities on a proportional or logarithmic scale rather than linear scale. Thus use of dB unit is more appropriate for representation of amplifier gains.

12. What is the coupling schemes used in multistage amplifiers? (May,10) [**CO2-L1**]

In multistage amplifier, the output signal of preceding stage is to be coupled to the input circuit of succeeding stage. For this interstage coupling, different types of coupling elements can be employed.

These are : 1. RC coupling
2. Transformer coupling
3. Direct coupling

13. Define Common Mode Rejection Ratio. (Nov, 09) [**CO2-L2**]

Common Mode Rejection Ratio is the figure of merit of a differential amplifier to reject common mode signal and is given by,

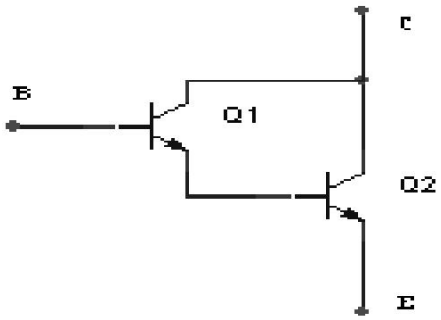
$$\text{CMRR} = \frac{\text{Gain of the amplifier for a difference mode input signal}}{\text{Gain of the amplifier for a common mode input signal}}$$

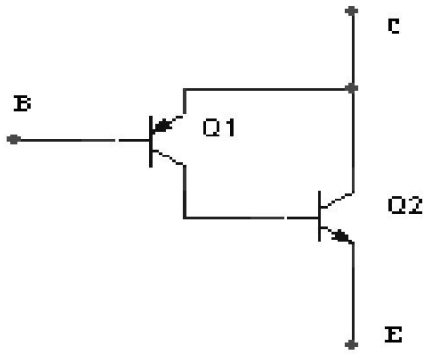
$$C = \left| \frac{A_d}{A_c} \right|$$

14. What does bootstrapping mean? Why bootstrapping is done in a buffer amplifier? (Nov, 10) [**CO2-L3**]

In the emitter follower amplifier A_V tends to unity. If a resistor is connected between input and output of the emitter follower, the change in the voltage at one end of the resistor changes the voltage at the other end of the resistor by same value. It is as if resistor is pulling itself up by its bootstraps. Such effect is known as *boot strapping.*

15. Draw the Darlington emitter follower circuit. (May,14,13) [**CO2-L3**]





16. How can a DC equivalent circuit of an amplifier be obtained? [**CO2-L2**]

The analysis of transistor circuits for small signal behavior can be made by following simple guidelines. These guidelines are,

- Draw the actual circuit diagram
- Replace coupling capacitors and emitter bypass capacitor by short circuit
- Replace D.C. source by a short circuit
- Mark the points B, E, C on the circuit diagram and locate these points as the start of the equivalent circuit
- Replace the transistor by its h-parameter model

17. State Miller's Theorem. (May,15) [**CO2-L1**]

It states that the effect of resistance Z on the input circuit is a ratio of input voltage to the current which flows from the input to the output.

$$Z_1 = \frac{Z}{1-K}$$

It states that the effect of resistance Z on the output circuit is the ratio of output voltage to the current which flows from the output to input.

$$Z_2 = \frac{Z-K}{K-1}$$

18. Define i) Differential gain ii) Common mode gain [**CO2-L1**]

The gain with which differential amplifier amplifies the difference between two input signals is called differential gain of the differential amplifier denoted as A_D. The gain with which it amplifies the common mode signal to produce the output is called common mode gain of the differential amplifier denoted as A_C.

19. What are practical limitations in selecting very high R_E? [**CO2-L2**]

- Large R_E needs higher biasing voltage to set the operating point of the transistors.
- This increases the overall chip area. Hence practically R_E can not be selected very high.

20. What are the limitations of h parameters? [**CO2-L1**]

The h parameters has the following limitations,

- The accurate calculation of h parameters is difficult.
- A transistor behaves as a two port network for small signals only, hence h parameters can be used to analyze only the small signal amplifiers.

21. What are the advantages of Darlington amplifier? [**CO2-L2**]

A Darlington transistor connection provides a transistor having a very large current gain, typically a few thousand. The main features of the Darlington connection is that the composite transistor acts as a single unit with a current gain that is the product of current gains of the individual transistors.

$$\beta D = \beta 1 \beta 2$$

βD = Darlington connection current gain

β1 and β2 – Current gain of the transistors 1 & 2 in the Darlington pair

22. Methods of coupling multistage amplifiers. [**CO2-L2]**

- RC coupling
- Transformer coupling
- Direct coupling

23. Features of differential amplifier, [**CO2-L1]**

- High differential voltage gain
- Low common mode gain
- High CMRR
- Two input terminals
- High input impedance
- Large bandwidth
- Low offset voltages and currents
- Low output impedance

24. List the configuration of differential amplifiers. [**CO2-L3]**

- Dual input, balanced output differential amplifier
- Dual input, unbalanced output differential amplifier
- Single input, balanced output differential amplifier
- Single input, unbalanced output differential amplifier

25. State Bisection Theorem. (Nov, 12) [**CO2-L1]**

A particular network which has mirror symmetry with respect to an imaginary line. If the entire network is denoted as N then it can be divided into two half networks N/2 about the line of symmetry is called bisection theorem or Bartlett's bisection theorem.

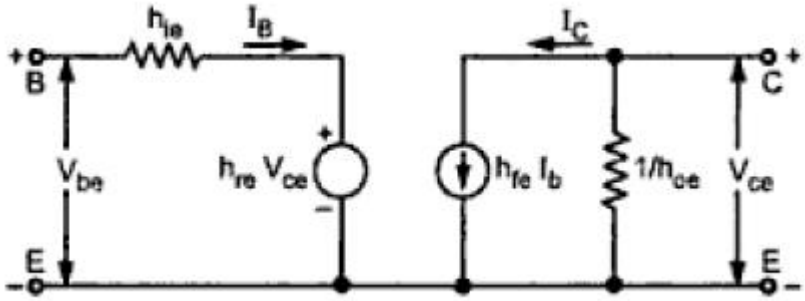
26. What are the other methods to improve CMRR without RE? [**CO2-L1]**

- Constant current bias method
- Current mirror circuit.

27. List the advantage of current mirror circuit? [**CO2-L1]**

- Provides very high emitter resistance RE.
- Requires fewer components than the constant current bias.
- Simple to design
- Easy to fabricate.
- With properly matched transistors, collector current thermal stability is achieved.

28. Draw the small signal equivalent circuit of CE amplifier. [**CO2-L3**]



28. Define Miller effect input capacitance.[Dec-2006, Dec2007, May-2008] [**CO2-L2**]

For any inverting amplifier, the input capacitance will be increased by a miller effect capacitance, sensitive to the gain of the amplifier and the inter electrode capacitance connected between the input and output terminals of the active device. CMi = (1- AV) Cf CM0 = Cf Cf = Inter electrode capacitance between input and output.

PART B

1. Explain about the Small Signal Low Frequency h-parameter Model of transistor amplifier. [**CO2-H1**]

Let us consider the transistor amplifier as a block box.

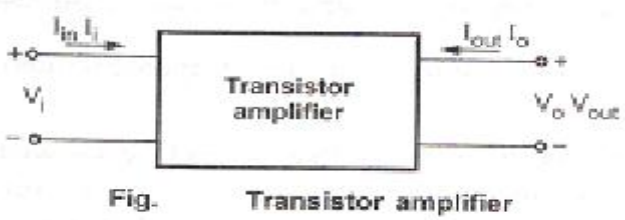


Fig. Transistor amplifier

Where, I_i – input current to the amplifier
V_i - input voltage to the amplifier
I_o – output current of the amplifier
V_o – output voltage of the amplifier
Input current is an independent variable. Input voltage and output current are dependent variables. Input current and output voltage are independent variables.

$$V_i = f_1(I_i, V_o)$$
$$I_o = f_2(I_i, V_o)$$

This can be written in the equation form as,

$$V_i = h_{11} I_i + h_{12} V_o$$
$$I_o = h_{21} I_i + h_{22} V_o$$

The above equation can also be written using alphabetic notations,

$$V_i = h_i \cdot I_i + h_r \cdot V_o$$
$$I_o = h_f \cdot I_i + h_o \cdot V_o$$

Definitions of h-parameter:

The parameters in the above equations are defined as follows

$$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0}$$
$$h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i=0}$$
$$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0}$$
$$h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0}$$

h_{11} – input resistance with output short-circuited in ohms
h_{12} – fraction of output voltage at input with input open circuited, it is unitless h_{21} – forward current transfer ratio or current gain with output short circuited, it is unitless
h_{22} – output admittance with input open circuited in mhos

Benefits of h-parameters:

1. Real numbers at audio frequencies
2. Easy to measure
3. Can be obtained from the transistor static characteristic curve
4. Convenient to use in circuit analysis and design
5. Most of the transistor manufacturers specify the h-parameters

h-Parameters for all three configurations:

Transistor can be represented as two port network by making anyone terminal common between input and output. There are three possible configurations in which a transistor can be used, there is a change in terminal voltage and current for different transistor configurations. To designate the type of configuration another subscript is added to h-parameters.

$h_{ie} = h_{11e}$– input resistance in CE configuration

$h_{fb} = h_{21b}$ – short circuit current gain in CB configuration

Table: Summarizes h-parameters for all three configurations

Parameter	CB	CE	CC
Input resistance	h_{ib}	h_{ie}	h_{ic}
Reverse voltage gain	h_{rb}	h_{re}	h_{rc}
Forward transfer current gain	h_{fb}	h_{fe}	h_{fc}
Output admittance	h_{ob}	h_{oe}	h_{oc}

The basic circuit of hybrid model is same for all three configurations, only parameters are different.

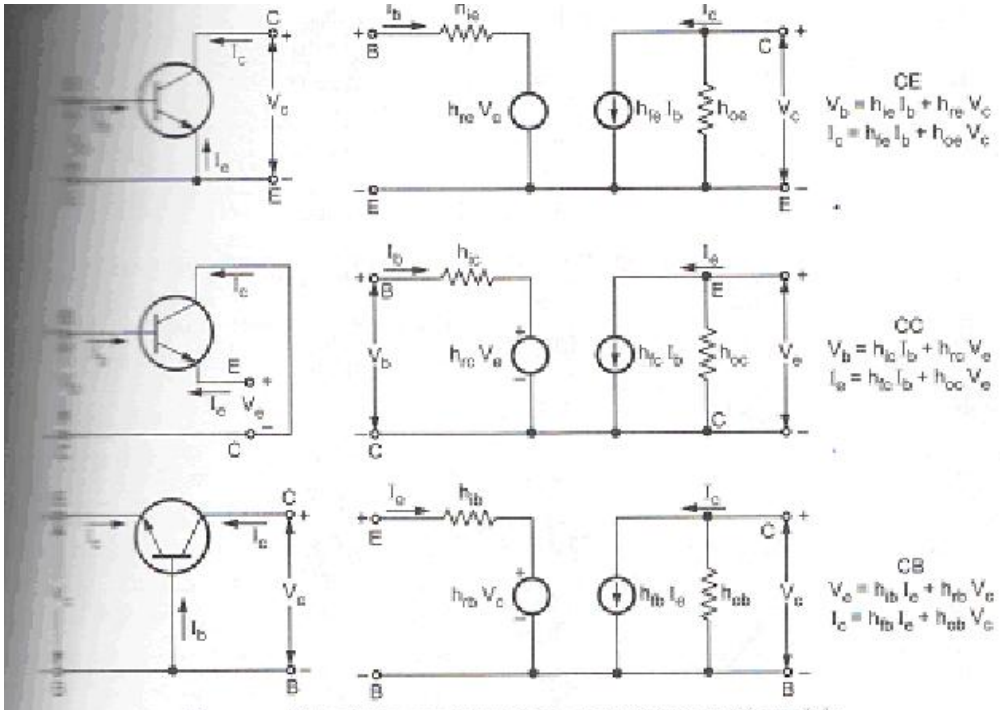


Fig. Transistor configurations and their hybrid models

The circuit and equations are valid for either NPN or PNP transistor and are independent of the type of load or method of biasing.

Determination of h-parameters from characteristics:

Consider CE configuration, its functional relationship can be defined from the following equations:

$$V_{be} = f_1 (I_b , V_{ce})$$
$$I_c = f_2 (I_b , V_{ce})$$

The input characteristic curve gives the relationship between input voltage V_{BE} and input current I_B for different values of output voltage V_{CE}. The following figure shows the typical input characteristic curve for CE configuration.

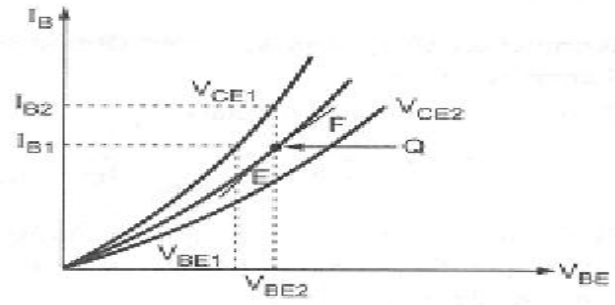


Fig. Typical input characteristic curves for the common emitter transistor configuration

Determination of h_{ie} and h_{re} from characteristic curve:

Parameter h_{ie}:

$$h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}\text{ constant}} = \frac{V_{BE2} - V_{BE1}}{I_{B2} - I_{B1}}$$

Parameter h_{re}:

$$h_{re} = \left.\frac{\Delta V_{BE}}{\Delta V_{CE}}\right|_{I_B\text{constant}} = \frac{V_{BE2} - V_{BE1}}{V_{CE2} - V_{CE1}}$$

The output characteristic curve gives the relationship between output current I_C and output voltage V_{CE} for different values of input current I_B.

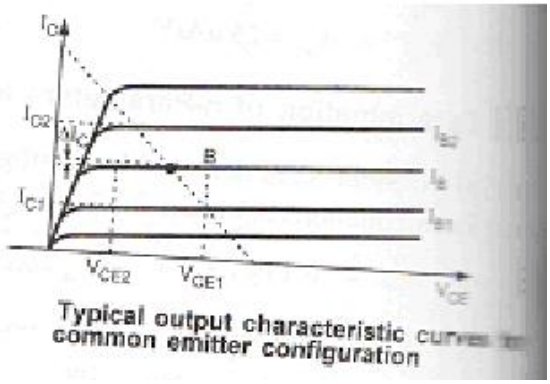


Fig. Typical output characteristic curves for common emitter configuration

Determination of h_{fe} and h_{oe} from output characteristic curve:

Parameter h_{fe}:

$$h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\text{ constant}} = \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}}$$

Parameter h_{oe}:

$$h_{oe} = \left.\frac{\Delta I_C}{\Delta V_C}\right|_{I_B\text{ constant}} = \frac{I_{C2} - I_{C1}}{V_{CE2} - V_{CE1}}$$

2. Detail about Mid band analysis of BJT Single Stage Amplifiers [CO2-H2]

Consider the basic amplifier circuit. To form a transistor amplifier only is is necessary to connect an external load and signal source along with proper biasing.

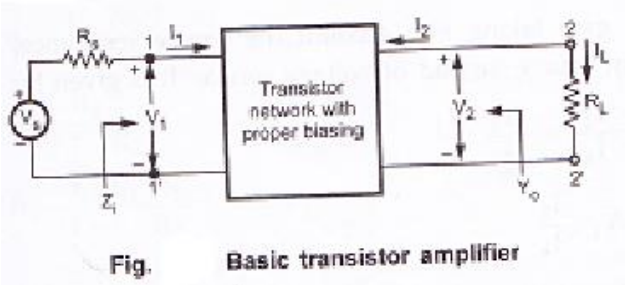


Fig. Basic transistor amplifier

We can replace the transistor circuit as shown in the following figure.

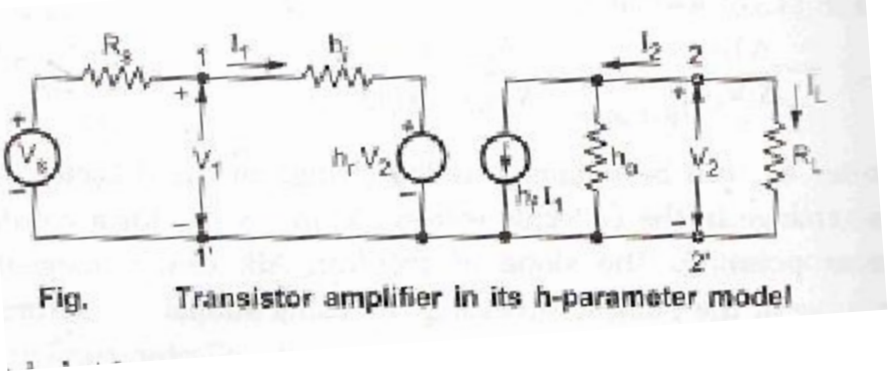


Fig. Transistor amplifier in its h-parameter model

Let us analyze the hybrid model to find current gain, input resistance, voltage gain and output resistance.

Current gain (A_i):

It is defined as the ratio of output to input current. It is given by,

$$A_i = \frac{I_L}{I_1} = -\frac{I_2}{I_1}$$

Here I_L and I_2 are equal in magnitude but opposite in sign. $I_L = -I_2$

From above circuit,

$$I_2 = h_f I_1 + h_o V_2$$

Substituting $V_2 = -I_2 R_L$ in the equation, then equation become,

$$I_2 = h_f I_1 + h_o (-I_2 R_L)$$

$$I_2 + h_o I_2 R_L = h_f I_1$$

$$(1 + h_o R_L) I_2 = h_f I_1$$

$$\frac{I_2}{I_1} = \frac{h_f}{1 + h_o R_L}$$

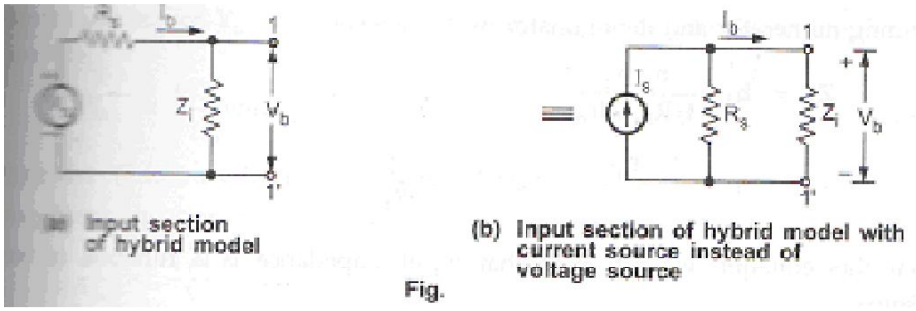
$$A_i = -\frac{I_2}{I_1} = \frac{-h_f}{1 + h_o R_L}$$

Current gain (A_{IS}):

It is given by,

$$A_{is} = -\frac{I_2}{I_s} = -\frac{I_2}{I_1} \cdot \frac{I_1}{I_s}$$

$$= A_i \cdot \frac{I_1}{I_s}$$



(a) Input section of hybrid model

(b) Input section of hybrid model with current source instead of voltage source

Fig.

From above figure, using current divider rule,

$$I_1 = \frac{I_s R_s}{Z_i + R_s}$$

$$\frac{I_1}{I_s} = \frac{R_s}{Z_i + R_s}$$

$$A_{is} = \frac{A_i R_s}{Z_i + R_s}$$

Input Impedance (Z_i):

R_i is the input resistance looking into the amplifier input terminals (1, 1'). It is given by,

$$R_i = \frac{V_1}{I_1}$$

From the input circuit,

$$V_1 = h_i I_1 + h_r V_2$$

$$Z_i = \frac{V_1}{I_1} = \frac{h_i I_1 + h_r V_2}{I_1}$$

$$Z_i = h_i + h_r \frac{V_2}{I_1}$$

Substituting $V_2 = -I_2R_L = A_i I_1 R_L$ in the above equation,

$$Z_i = h_i + \frac{h_r A_i I_1 R_L}{I_1} = h_i + h_r A_i R_L$$

Substituting

$$A_i = -\frac{h_f}{1 + h_o R_L}$$

Then we get,

$$Z_i = h_i - \frac{h_r h_f R_L}{1 + h_o R_L}$$

Dividing numerator and denominator by R_L we get,

$$Z_i = h_i - \frac{h_r h_f}{1/R_L + h_o}$$

$$Z_i = h_i - \frac{h_r h_f}{Y_L + h_o} \quad \text{where } Y_L = \frac{1}{R_L}$$

From this equation, note that the input impedance is a function offload impedance.

Voltage gain (A_v):

It is the ratio of output voltage to input voltage. It is given by,

$$A_v = \frac{V_2}{V_1}$$

By substituting $V_2 = -I_2R_L = A_i I_1 R_L$

$$A_v = \frac{A_i I_1 R_L}{V_1} = \frac{A_i R_L}{Z_i}$$

$$\frac{I_1}{V_1} = \frac{1}{Z_i}$$

Voltage gain (A_{vs}):

It is voltage gain including the source. It is given by,

$$A_{vs} = \frac{V_2}{V_S} = \frac{V_2}{V_1} \times \frac{V_1}{V_S}$$

$$A_{vs} = A_v \times \frac{V_1}{V_S}$$

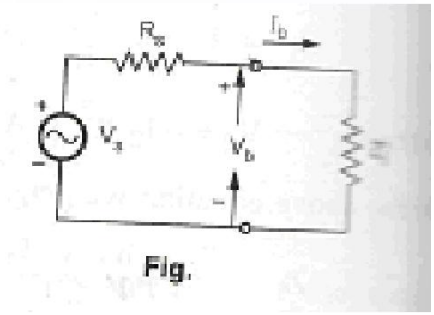


Fig.

From above figure, applying potential divider rule, then we get,

$$V_1 = \frac{Z_i}{R_s + Z_i} V_S$$

$$\frac{V_1}{V_S} = \frac{Z_i}{R_s + Z_i}$$

Substituting the value of V_1/V_s in the equation of

$$A_{vs} = A_v \times \frac{V_1}{V_S}$$

We get,

$$A_{vs} = A_v \cdot \frac{Z_i}{R_s + Z_i}$$

$$= \frac{A_i R_L}{R_s + R_i} \quad \because A_v = \frac{A_i R_L}{Z_i}$$

Output Admittance (Y_o):

It is the ratio of output current to output voltage. It is given by,

$$Y_o = \frac{I_2}{V_2} \text{ with } V_s = 0$$

From equation,

$$I_2 = h_f I_1 + h_o V_2$$

Dividing above equation by V_2, We get,
From transistor amplifier in h-parameter model circuit, with $V_s = 0$,

$$\frac{I_2}{V_2} = \frac{h_f I_1}{V_2} + h_o$$

$$Y_o = h_f \frac{I_1}{V_2} + h_o$$

$R_s I_1 + h_i I_1 + h_r V_2 =$
$0 \; (R_s + h_i) \; I_1 = -h_r$
V_2

$$\frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i}$$

Substituting the value of I_1/V_2 from above equation in the equation of Y_o, We obtain,

$$Y_o = h_o - \frac{h_f h_r}{h_i + R_s}$$

From this equation, note that the output admittance is a function of source resistance.

Power gain (Ap):

It is the ratio of average power delivered to the load to the input power.
Output power is given as,

$$P_2 = V_2 I_L = -V_2 I_2$$

Since the input power is $P_1 = V_1 I_1$
The operating power gain A_p of the transistor is given as,

$$A_p = \frac{P_2}{P_1} = -\frac{V_2 I_2}{V_1 I_1} = A_v A_i = A_i^2 \frac{R_L}{Z_i} \quad \because A_v = \frac{A_i R_L}{Z_i}$$

Relation between A_{vs} and A_{IS}:
From equation,

$A_{vs} = \frac{A_i R_L}{R_s + R_i} \quad \because A_v = \frac{A_i R_L}{Z_i}$ and $A_{is} = \frac{A_i R_s}{Z_i + R_s}$

We have,

$$A_{vs} = \frac{A_i R_L}{Z_i + R_s} \quad \& \quad A_{is} = \frac{A_i R_s}{Z_i + R_s}$$

Taking ratio of above two equations we get,

$$\frac{A_{vs}}{A_{is}} = \frac{R_L}{R_s}$$

$$A_{vs} = A_{is} \cdot \frac{R_L}{R_s}$$

Table: Summarizes small signal analysis of a transistor amplifier

$A_i = \frac{h_f}{1+h_o R_L}$
$A_{is} = \frac{A_i R_s}{Z_i + R_s}$
$Z_i = h_i + h_r A_i R_L = h_i - \frac{h_f h_r}{h_o + Y_L}$
$A_v = \frac{A_i R_L}{Z_i}$
$A_{VS} = \frac{A_v R_i}{Z_i + R_s} = \frac{A_i R_L}{Z_i + R_s} = \frac{A_{is} R_L}{R_s}$
$Y_o = h_o - \frac{h_f h_r}{h_i + R_s} = \frac{1}{Z_o}$
$A_P = A_V A_i = A_i^2 \frac{R_L}{Z_i}$

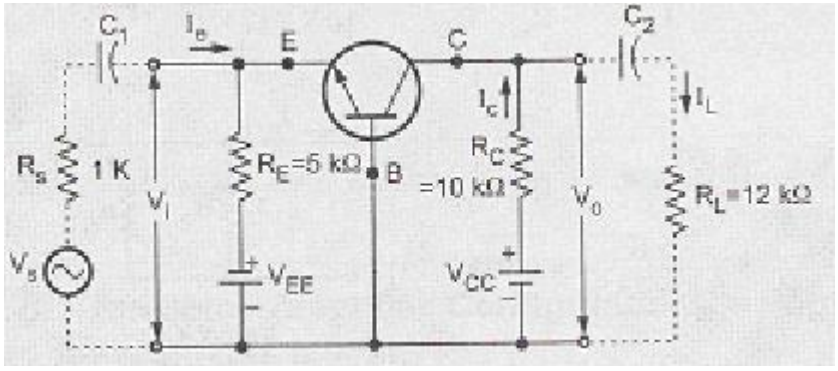
Method for analysis of a transistor circuit:

The analysis of transistor circuits for small signal behaviour can be made by following simple guidelines. These guidelines are,

- Draw the actual circuit diagram

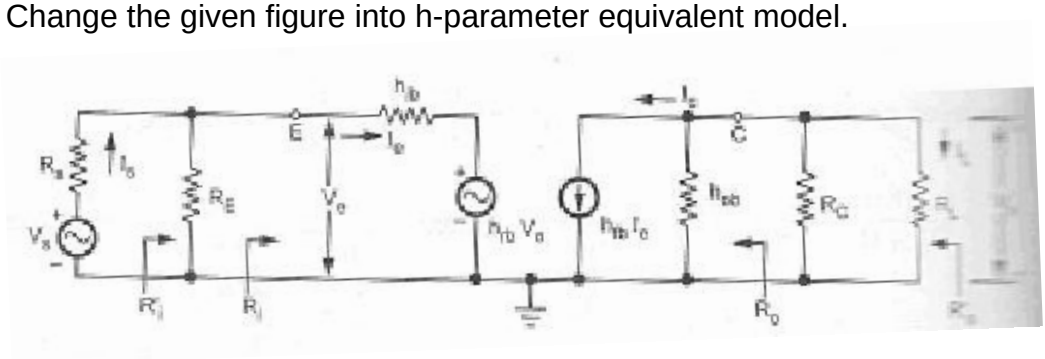
- Replace coupling capacitors and emitter bypass capacitor by short circuit
- Replace D.C. source by a short circuit
- Mark the points B, E, C on the circuit diagram and locate these points as the start of the equivalent circuit
- Replace the transistor by its h-parameter model

3. For the common base circuit shown in figure, transistor parameters are h_{ib} = 22Ω,h_{fb} = -0.98, h_{ob} = 0.49μA/V, h_{rb} = 2.9*10 $^{-4}$. Calculate the values of input resistance, output resistance, current gain and voltage gain for the given circuit. [**CO2-H2**]



Solution:

Change the given figure into h-parameter equivalent model.



a) Current gain

$$(A_i) = -\frac{h_{fb}}{1+h_{ob}R'_L} = \frac{-(-0.98)}{1+0.49\times10^{-6}\times5.45\,K} = 0.977$$

b) Input Resistance

$$(R_i) = h_{ib} + h_{rb}\,A_i\,R'_L$$
$$= 22\,\Omega + 2.9\times10^{-4}\times(0.977)\,(5.45\,K) = 23.54\,\Omega$$
$$R'_i = R_i \parallel R_E = 23.54 \parallel 5\,K = \mathbf{23.43}\,\Omega$$

c) Voltage gain

$$(A_v) = \frac{A_i R'_L}{R_i} = \frac{(0.977)\times(5.45\,K)}{23.54} = 226$$

d) Overall voltage gain

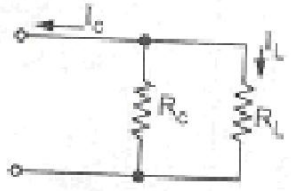
$$A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_e} \times \frac{V_e}{V_s} \quad \text{where } \frac{V_o}{V_e} = A_v \quad \frac{V_e}{V_s} = \frac{R_i'}{R_i' + R_s}$$

$$A_{vs} = A_v \frac{R_i'}{R_i' + R_s} = 226 \times \frac{23.43}{20.36 + 1\,K} = 5.174$$

e) Overall current gain

$$A_i = \frac{I_L}{I_s} = \frac{I_L}{I_c} \times \frac{I_c}{I_e} \times \frac{I_e}{I_s}$$

$$\frac{I_L}{I_c} = -\frac{R_C}{R_C + R_L} = -\frac{10\,K}{10\,K + 12\,K} = -0.454$$



Fig

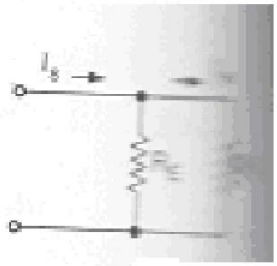


Fig.

$$\frac{I_c}{I_e} = -A_i = -0.977$$

$$\frac{I_e}{I_s} = \frac{R_E}{R_E + R_i} = \frac{5\,K}{5\,K + 23.54} = 0.995$$

$$\therefore A_{i(\text{for circuit})} = (-0.454) \times (-0.977) \times 0.996 = 0.441$$

f) Output Resistance

$$(R_o) = \frac{1}{h_{ob} - \frac{h_{fb} h_{rb}}{h_{ib} + R_s'}}$$

$$= \frac{1}{0.49 \times 10^{-6} - \left(\frac{-0.98 \times 2.9 \times 10^{-4}}{22 + 833.33}\right)} = 1.21\ M\Omega$$

$R_o' = R_o \,||\, R_L' = 1.21M \,||\, 5.45K = 5.425K\Omega$

Problem 2: Consider a single stage CE amplifier with R_s = 1KΩ, R_L = 1.2KΩ. Calculate A_i, R_i,
A_v, A_{is}, power gain and R_o if h_{ie} = 1.1k, $h_{re} = 2.5*10^{-4}$, h_{fe} = 50 and h_{oe} = 25μA/V.
[**CO2-H2]**

Solution:

Ai = $$\frac{-h_{fe}}{1+h_{oe}R_L} = \frac{-50}{1+25\times10^{-6}\times1.2\times10^{3}} = -48.54$$

R_i = $$h_{ie}+h_{re}A_i R_L = 1100 - 2.5\times10^{-4}\times 48.54 \times 1200 = 1085.44\ \Omega$$

A_v = $$\frac{A_i R_L}{R_i} = \frac{-48.54\times 1200}{1085.44} = -53.663$$

A_{vs} = $$\frac{A_v R_i}{R_i+R_s} = -\frac{53.663\times 1085.44}{1085.44+1000} = -27.93$$

A_{is} = $$\frac{A_i R_s}{R_i+R_s} = -\frac{48.54\times 1000}{1085.44+1000} = -23.28$$

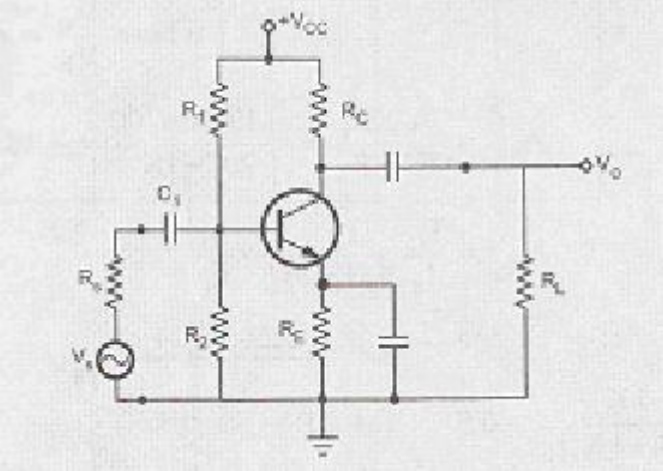
$$h_{oe} - \frac{h_{fe}h_{re}}{h_{ie}+R_s} = 25\times10^{-6} - \frac{50\times 2.5\times10^{-4}}{1100+1000} = 19.0\ \mu A/V$$

Y_o =

$$\frac{1}{Y_o} = \frac{1}{19\times10^{-6}} = 52.6\ K$$

Problem 3:

Consider a single stage CE amplifier with R_s = 1k, R_1 = 50k, R_2 = 2k, R_c = 2k, R_L = 2K, h_{ie} = 1.1k, h_{oe} = 25µA/V, h_{fe} = 50 and h_{re} = 2.5*10^{-4} as shown in the figure.
Find Ai, R_i, A_v, A_i, A_{vs} and R_o. [**CO2-H3]**



Solution:
Since h_{oe} R_L' = 25*10^{-6}*(2K || 2K) = 0.25, which is less than 0.1, so use approximate analysis.
Consider the simplified hybrid model for the given circuit.

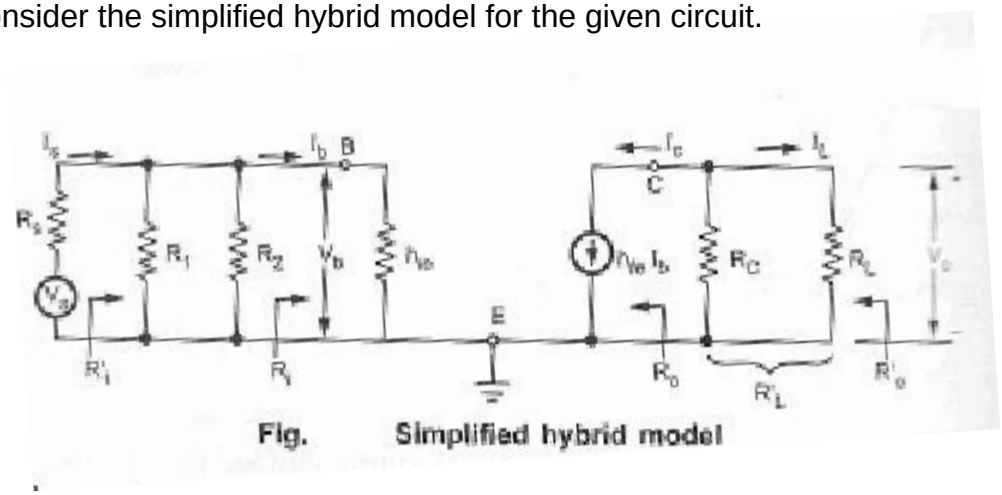


Fig. Simplified hybrid model

a) Current gain

$$(A_v) = \frac{A_i R_L}{R_i} = \frac{-50\times(2K\|2K)}{1.1K} = -45.45$$

b) Input Impedance

$$(R_i) = h_{ie} = 1.1\ K$$

$$R_i' = h_{ie} \| R_1 \| R_2 = 1.1\ K \| 50\ K \| 2\ K = 700\ \Omega$$

$$(A_i) = -h_{fe} = -50$$

c) Output Impedance

$$(R_o) = \frac{1}{Y_o} = \infty$$

d) Overall voltage gain

$$R'_o = R_o \parallel R'_L = \infty \parallel 2\,K \parallel 2\,K = 1\,K$$

$$(A_{vs}) = \frac{V_o}{V_s} = \frac{V_o}{V_b} \times \frac{V_b}{V_s}$$

$$A_{vs} = \frac{A_v R'_i}{R'_i + R_s} = \frac{-45.45 \times 700}{700 + 1K} = -18.71$$

e) Overall current gain

$$A_i = \frac{I_L}{I_s} = \frac{I_L}{I_C} \times \frac{I_C}{I_b} \times \frac{I_b}{I_s}$$

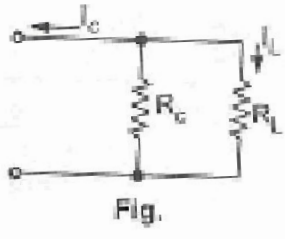


Fig.

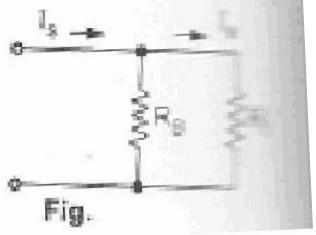


Fig.

$$\frac{I_L}{I_c} = -\frac{R_C}{R_C + R_L} = \frac{-1K}{1K + 1K} = -0.5$$

$$\frac{I_c}{I_b} = h_{fe} = 50$$

Comparison of Transistor Configurations:

Sr.No.	Characteristic	Common Base	Common Emitter	Common Collector
1.	Input resistance	Very low (20 Ω)	Low (1 kΩ)	High (500 kΩ)
2.	Output resistance	Very high (1 MΩ)	High (40 kΩ)	Low (50 Ω)
3.	Input current	I_E	I_B	I_B
4.	Output current	I_C	I_C	I_E
5.	Input voltage applied between	Emitter and Base	Base and Emitter	Base and Collector
6.	Output voltage taken between	Collector and Base	Collector and Emitter	Emitter and Collector
7.	Current amplification factor	$\alpha = \frac{I_C}{I_E}$	$\beta = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$
8.	Current gain	Less than unity	High (20 to few hundreds)	High (20 to few hundreds)
9.	Voltage gain	Medium	Medium	Low
10.	Applications	As a input stage of multistage amplifier	For audio signal amplification	For impedance matching

13. Explain briefly about differential amplifier and derive its expressions. [CO2-H2]

A device which accepts an input signal and produces an output signal proportional to the input, is called an amplifier. An amplifier which amplifies the difference between the two input signals is called differential amplifier. The differential amplifier configuration is used in variety of analog circuits. The. differential amplifier is an essential and basic building block in modern IC amplifier .The Integrated Circuit (IC)technology is well known now a days, due to which the design of complex circuits become very simple. The IC version of operational amplifier is inexpensive, takes up less space and consumes less power. The. differential amplifier is the basic building block of such IC operational amplifier.

Basics of Differential Amplifier

The Differential Amplifier amplifies the difference between two input voltage signal. Hence it is also called as difference amplifier.

Consider an ideal differential amplifier shown in the Fig. A

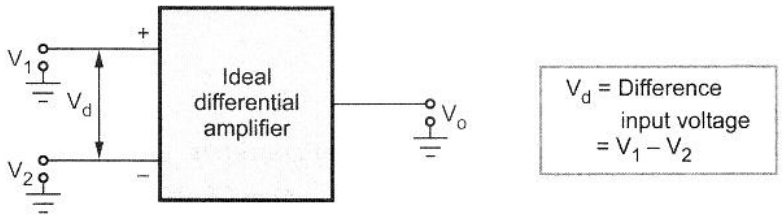


Fig. Ideal differential amplifier

V_1 and V_2 are the two input signals while Vo is the output. Each signal is measured with respect to the ground. In an ideal differential amplifier, the output voltage Vo is proportional to the difference between the two input signals. Hence

we can write,

$$V_o \propto (V_1 - V_2) \quad \ldots(1)$$

Differential Gain A_d

From Equation 1 we can write,

$$\therefore \quad V_o = A_d (V_1 - V_2) \quad \ldots(2)$$

where A_D is the constant of proportionality. The A_D is the gain with which differential amplifier amplifies the difference between two input signals. Thus it is called differential gain of the differential amplifier.

Thus, Ad = Differential gain.The difference between the two inputs (V_1 - V_2) is generally called difference voltage and denoted as Vd.

$$V_o = A_d V_d \quad \ldots(3)$$

Hence the differential gain can be expressed as,

$$A_d = \frac{V_o}{V_d} \quad \ldots(4)$$

Generally the differential gain is expressed in its decibel (dB) value as,

$$A_d = 20 \text{ Log}_{10} (A_d) \text{ in dB} \quad \ldots(5)$$

Common Mode Gain Ac

If we apply two input voltages which are equal in all the respects to the differential amplifier i.e. V1 = Vz then ideally the output voltage Vo = (V_1 - V_2) A_d, must be zero.But the output voltage of the practical differential amplifier not only depends on thedifference voltage but also depends on the average common level of the two inputs.Such an average level of the two input signals is called common mode signal denoted as V_C

$$V_c = \frac{V_1 + V_2}{2} \quad \ldots(6)$$

Practically, the differential amplifier produces the output voltage proportional to such common mode signal, also. The gain with which it amplifies the common mode signal to produce the output is called common mode gain of the differential amplifier $A_{C.\backslash}$

$$V_o = A_c V_c \quad ..(7)$$

Thus there exists some finite output for V1 = V2 due to such common mode gain A_C, in case of practical differential amplifiers.

So the total output of any differential amplifier can be expressed as,

$$V_o = A_d V_d + A_c V_c \quad ..(8)$$

For an ideal differential amplifier, the differential gain A_d, must be infinite while the common mode gain must be zero.

But due to mismatch in the internal circuitry, there is some output available for V_1 = V2 and gain A_C is not practically zero. The value of such common mode gain A_C very small while the value of the differential gain A_d is always very large.

Common Mode Rejection Ratio (CMRR)

When the same voltage is applied to both the inputs, the differential amplifier is said to be operated in a common mode configuration. Many disturbance signals, noise signal appear as a common input signal to both the input terminals of the differential amplifier. Such a common signal should be rejected by the differential amplifier. The ability of a differential amplifier to reject a common mode signal is expressed by a ratio called common mode rejection ratio denoted as CMRR. It is defined as the ratio of the differential voltage gain A_d to common mode voltage gain A_C

$$\text{CMRR} = \rho = \left|\frac{A_d}{A_c}\right| \quad ....(9)$$

$$\text{CMRR in dB} = 20 \log \left|\frac{A_d}{A_c}\right| \text{dB} \quad .....(10)$$

14. Discuss about Common Mode Operation. [**CO2-H2]**

In this mode, the signals applied to the base of Q1 and Q2 are derived from the same source. So the two signals are equal in magnitude as well as in phase. The circuit diagram is shown in the Fig.

In phase signal voltages at the bases of Q1 and Q2 causes in phase signal voltages to appear across R_E, which add together. Hence R_E carries a signal current and provides a negative feedback. This feedback reduces the common mode gain of differential amplifier.

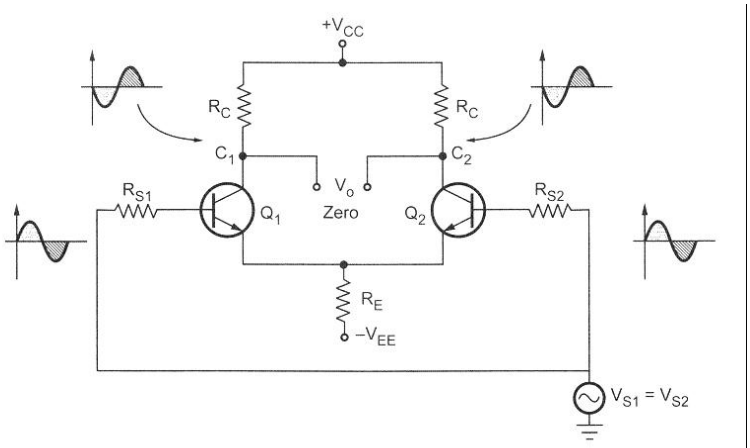


Fig. Common mode operation

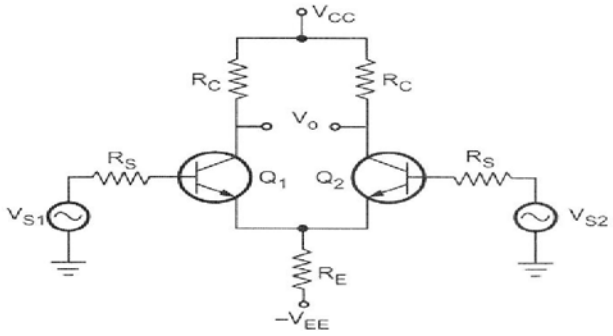
While the two signals causes in phase signal voltages of equal magnitude to appear across the two collectors of Q_1 and Q2. Now the output voltage is the difference between the two collector voltages, which are equal and also same in phase, Eg. (20) - (20) = 0. Thus the difference output Vo is almost zero, negligibly small. ideally it should be zero.

Configurations of Differential Amplifier

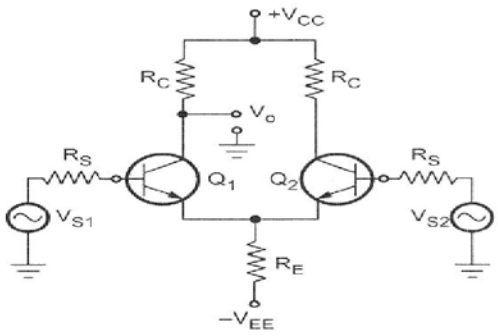
The differential amplifier, in the difference amplifier stage in the op-amp, can be used in four configurations :

- Dual input balanced output differential amplifier.
- Dual input, unbalanced output differential amplifier.
- Single input, balanced output differential amplifier.
- Single input, unbalanced output differential amplifier.

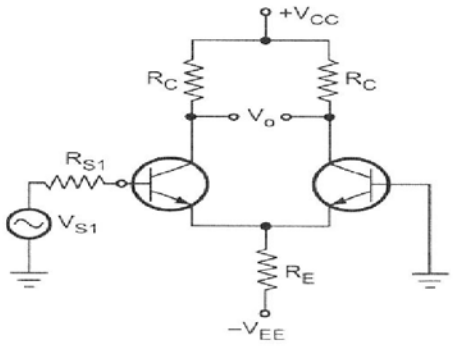
The differential amplifier uses two transistors in common emitter configuration. If output is taken between the two collectors it is called balanced output or double ended output. While if the output is taken between one collector with respect to ground it is called unbalanced output or single ended output. If the signal is given to both the input terminals it is called dual input, while if the signal is given to only one input terminal and other terminal is grounded it is called single input or single ended input. Out of these four configurations the dual input, balanced output is the basic differential amplifier configuration. This is shown in the Fig. (a). The dual input, unbalanced output differential amplifier is shown in the Fig.(b). The single input, balanced output differential amplifier is shown in the Fig (c) and the single input, unbalanced output differential amplifier is shown in the Fig. (d).



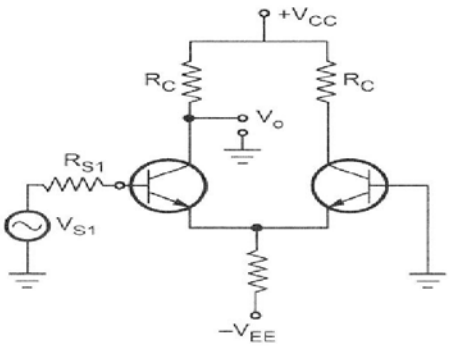
(a) Dual input balanced output



(b) Dual input unbalanced output



(c) Single input balanced output



(d) Single input unbalanced output

D.C. Analysis of Differential Amplifier

The d.c. analysis means to obtain the operating point values i.e. I_{CQ} and V_{CEQ} for the transistors used. The supply voltages are d.c. while the input signals are a.c., so d.c equivalent circuit can be obtained simply by reducing the input a.c. signals to zero. The d.c. equivalent circuit thus obtained is shown in the Fig.. Assuming $Rs_1 = R_{S2}$, the source resistance is simply denoted by

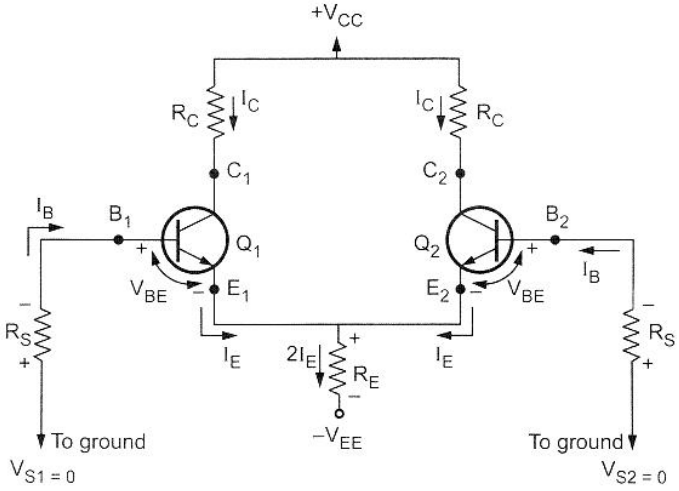


Fig. D.C. equivalent circuit

The transistors Q1 and Q_2 are matched transistors and hence for such a matched pair we can assume :

i) Both the transistors have the same characteristics.
ii) $R_{E1} = R_{E2}$ hence $R_E = R_{E1} \parallel R_{E2}$.

iii) $R_{C1} = R c_2$ hence denoted as R_C.

iv) $|V_{CC}| = |V_{EE}|$ and both are measured with respect to ground.

As the two transistors are matched and circuit is symmetrical, it is enough to find out operating point I_{CQ} and V_{CEQ}, for any one of the two transistors. The same is applicable for the other transistor.

Apply-g KVL to base-emitter loop of the transistor Q1,

$$-I_B R_S - V_{BE} - 2I_E R_E + V_{EE} = 0 \quad \text{....(1)}$$

$$I_C = \beta I_B \text{ and } I_C \cong I_E$$

$$I_B = \frac{I_E}{\beta} \quad \text{....(2)}$$

Substituting in equation (1), we get

$$\frac{-I_E R_S}{\beta} - V_{BE} - 2I_E R_E + V_{EE} = 0 \quad \text{....(3)}$$

$$I_E \left[\frac{-R_S}{\beta} - 2R_E\right] + V_{EE} - V_{BE} = 0 \quad \text{... (4)}$$

$$I_E = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E} \quad \text{... (5)}$$

V_{BE} = 0.6 to 0.7 V for silicon
= 0.2 V for germanium transistors.

In practice, generally $\frac{R_S}{\beta} << 2 R_E$

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E} \quad ...(6)$$

Now let us determine V_{CE}. As I_E is known and $I_E \cong I_C$, we can determine the collector voltage of Q_1 as

$$V_C = V_{CC} - I_C R_C \quad ...(7)$$

Neglecting the drop across R_S, we can say that the voltage at the emitter of Q_1 is approximately equal to $-V_{BE}$. Hence the collector to emitter voltage is

$$V_{CE} = V_C - V_E = (V_{CC} - I_C R_C) - (-V_{BE})$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C \quad ...(8)$$

Hence $I_E = I_C = I_{CQ}$ while $V_{CE} = V_{CEQ}$ for given values of V_{CC} and V_{EE}.

Thus for both the transistors, we can determine operating point values, using equations (6) and (8) With the same biasing arrangement, the d.c. analysis remains same for all the four possible configurations of differential amplifier.

$$I_E = \frac{V_{EE} - V_{BE}}{\frac{R_s}{\beta} + 2R_E} \approx \frac{V_{EE} - V_{BE}}{2R_E} \approx I_{CQ}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_{CQ} R_C$$

15. Important aspects of A.C. Analysis of Differential Amplifier using h-Parameters [CO2-H2]

In the a.c. analysis, we will calculate the differential gain A_d, common mode gain A_C, input resistance Ri and the output resistance R_0 of the differential amplifier circuit, using the h-parameters.

1. Differential Gain (A_d)

For the differential gain calculation, the two input signals must be different from each other. Let the two a.c. input signals be equal in magnitude but having 180" phase difference in between them. The magnitude of each a.c. input voltage V_{S1} and V_{S2} beVs /2. The two a.c. emitter currents I e_1 and I e_2 are equal in magnitude and 180' out of phase. Hence they cancel each other to get resultant a.c. current through the emitter as zero. For the a.c. purposes emitter terminal can be grounded. The a.c. small signal differential amplifier circuit with grounded emitter terminal is shown in the Fig1 As the two transistors are matched, the a.c. equivalent circuit for the other transistor is identical to the one shown in the Fig..1.

Thus the circuit can be analyzed by considering only one transistor. This is called as half circuit concept of analysis. The approximate hybrid model for the above circuit can be shown as in the Fig.2, neglecting ho_e,

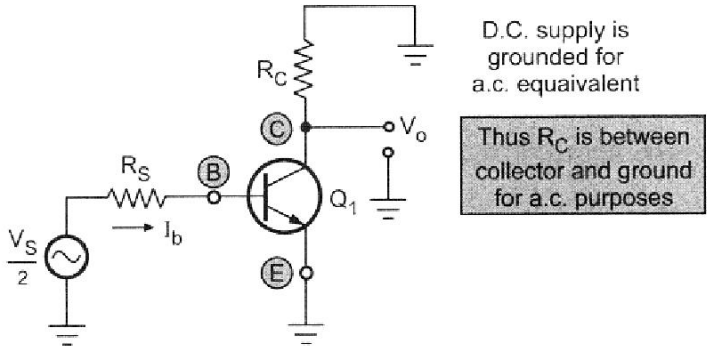


Fig.1 A.C. equivalent for differential operation

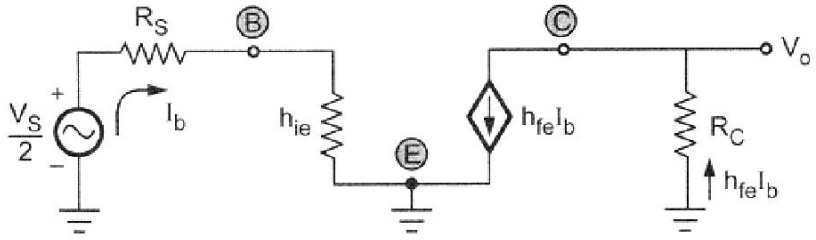


Fig.2 Approximate hybrid model

Applying KVL to the input loop,

$$-I_b R_S - I_b h_{ie} + \frac{V_S}{2} = 0 \qquad \ldots(1)$$

$$-I_b(R_S + h_{ie}) = -\frac{V_S}{2}$$

$$I_b = \frac{V_S}{2(R_S + h_{ie})} \qquad \ldots(2)$$

Applying KVL to the output loop,

$$V_o = -h_{fe} I_b R_C \qquad \ldots(3)$$

Substituting equation (2) in equation (3),

$$V_o = -h_{fe} R_C \frac{V_S}{2(R_S + h_{ie})}$$

$$\frac{V_o}{V_S} = \frac{-h_{fe} R_C}{2(R_S + h_{ie})} \qquad \ldots(4)$$

The negative sign indicates the phase difference between input and output. Now two input signal magnitudes are V_S /2 but they are opposite in polarity, as 180" out of phase.

$$V_d = V_1 - V_2 = \frac{V_S}{2} - \left(-\frac{V_S}{2}\right) = V_S$$

The **magnitude** of the differential gain A_d is

$$A_d = \frac{V_o}{V_S} = \frac{h_{fe} R_C}{2(R_S + h_{ie})} \quad \text{(For unbalanced output)} \qquad \ldots(5)$$

where V_S = Differential input

the expression for A_d with balanced output changes as

$$A_d = 2 \times \frac{h_{fe} R_C}{2(R_S + h_{ie})}$$

$$A_d = \frac{h_{fe} R_C}{(R_S + h_{ie})} \text{ (magnitude)} \qquad \ldots 6)$$

This is the differential gain for balanced output dual input differential amplifier circuit.

2. Common Mode Gain (A_C)

Let the magnitude of both the a.c. input signals be VS and are in phase with each other. Hence the differential input Vd = 0 while the common mode input Vc is the average value of the two.

$$V_c = \frac{V_1 + V_2}{2} = \frac{V_S + V_S}{2} \qquad \ldots(7)$$

$$= V_S$$

the output can be expressed as

$$V_o = A_c V_S \qquad \ldots (8)$$

$$A_c = \frac{V_o}{V_S} \qquad \ldots(.8\ (a))$$

But now both the emitter currents flows through R_E in the Same direction. Hence the total current flowing through R_E is $2I_e$. considering only one transistor, as in the Fig

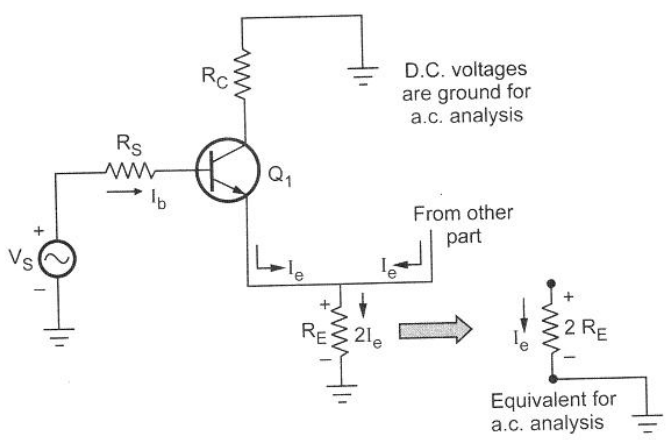


Fig. A.C. equivalent for common mode operation

The emitter resistance is shown 2 RE in the Fig

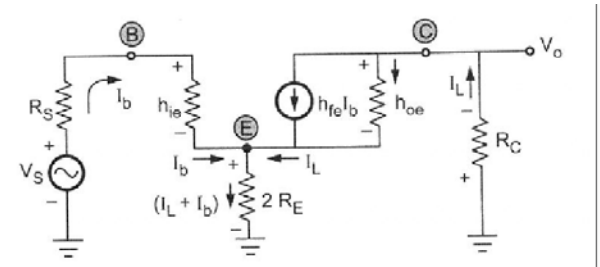


Fig. Approximate hybrid model

Current through R_C = Load current I_L

Effective emitter resistance = $2\ R_E$

Current through emitter resistance = $I_L + I_b$

Current through h_{oe} = $(I_L - h_{fe}\ I_b)$

Negative sign due to the assumed direction of current. Applying KVL to the output loop,

$$\frac{-(I_L - h_{fe}\ I_b)}{h_{oe}} - 2\ R_E\ (I_L + I_b) - I_L\ R_C = 0$$

$$\therefore \quad -\frac{I_L}{h_{oe}} + \frac{h_{fe}}{h_{oe}} I_b - 2R_E I_L - 2R_E I_b - I_L R_C = 0$$

$$I_b \left[\frac{h_{fe}}{h_{oe}} - 2R_E\right] = I_L \left[\frac{1}{h_{oe}} + 2R_E + R_C\right]$$

$$I_b [h_{fe} - 2R_E h_{oe}] = I_L [1 + h_{oe} (2R_E + R_C)]$$

$$\frac{I_L}{I_b} = \frac{[h_{fe} - 2R_E h_{oe}]}{[1 + h_{oe} (2R_E + R_C)]} \quad \ldots (10)$$

Substituting value of I_b, into the equation (8(b)), we get

$$V_S = \frac{I_L [1 + h_{oe} (2R_E + R_C)] (R_S + h_{ie} + 2R_E)}{[h_{fe} - 2R_E h_{oe}]} + I_L (2R_E)$$

$$\therefore \quad \frac{V_S}{I_L} = \frac{[1 + h_{oe} (2R_E + R_C)] (R_S + h_{ie} + 2R_E)}{[h_{fe} - 2R_E h_{oe}]} + (2R_E)$$

Finding L.C.M. and adjusting the terms, we get

$$\therefore \quad \frac{V_S}{I_L} = \frac{2R_E (1 + h_{fe}) + R_S (1 + 2R_E h_{oe}) + h_{ie} (1 + 2R_E h_{oe}) + h_{oe} R_C [2R_E + R_S + h_{ie}]}{[h_{fe} - 2R_E h_{oe}]}$$

$$\therefore \quad \frac{V_S}{I_L} = \frac{2R_E (1 + h_{fe}) + (R_S + h_{ie}) (1 + 2R_E h_{oe}) + h_{oe} R_C [2R_E + R_S + h_{ie}]}{[h_{fe} - 2R_E h_{oe}]} \quad \ldots (11)$$

Neglecting the terms of $h_{oe} R_C$ as practically $h_{oe} R_C << 1$.

$$\therefore \quad \frac{V_S}{I_L} = \frac{2R_E (1 + h_{fe}) + (R_S + h_{ie}) (1 + 2R_E h_{oe})}{[h_{fe} - 2R_E h_{oe}]} \quad \ldots (12)$$

Substituting the value of I_L, in the equation (9)

$$V_o = \frac{-V_S (h_{fe} - 2R_E h_{oe}) R_C}{2R_E (1 + h_{fe}) + (R_S + h_{ie}) (1 + 2R_E h_{oe})}$$

Hence the common mode gain can be written as (absorbing negative sign),

$$A_c = \frac{V_o}{V_S} = \frac{(2R_E h_{oe} - h_{fe}) R_C}{2R_E (1 + h_{fe}) + (R_S + h_{ie}) (1 + 2R_E h_{oe})} \quad \ldots (13)$$

In practice h_{oe} is generally neglected hence the expression for A_c can be further modified as

$$\therefore \quad \boxed{A_c = \frac{-h_{fe} R_C}{R_S + h_{ie} + 2R_E (1 + h_{fe})}} \quad \ldots (14)$$

Common Mode rejection Ratio (CMRR)

Once the differential and common mode gains are obtained, the expression for the CMRR can be obtained as,

$$CMRR = \left|\frac{A_d}{A_c}\right|$$

$$\therefore \quad CMRR = \frac{R_S + h_{ie} + 2R_E(1 + h_{fe})}{(R_S + h_{ie})} \qquad \ldots(15)$$

This is CMRR for **dual input balanced output** differential amplifier circuit.

Techniques of Improving Input Impedance

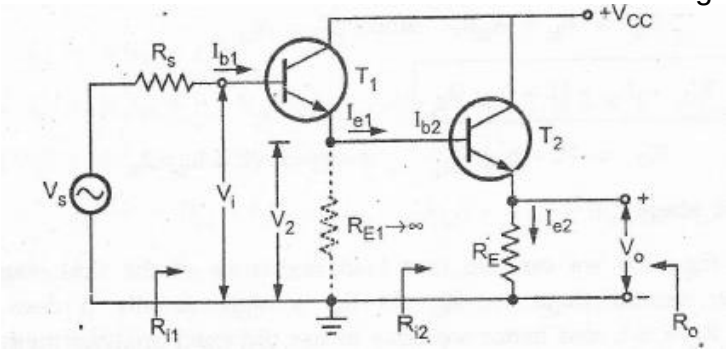
Among three configurations (CB, CC and CE), common collector or emitter follower circuit has high input impedance. Typically it is 200 KΩ to 300 KΩ. A single stage emitter follower circuit can give input impedance upto 500 KΩ. However, the input impedance considering biasing resistors is

Figure shows the direct coupling of two stages of emitter follower significantly less. Because Ri' = R_1 ll R_2 ll Ri The input impedance of the circuit can be improved by direct coupling of two stages of emitter follower amplifier. The input impedance can be increased using two techniques :

- Using direct coupling (Darlington connection)
- Using Bootstrap technique

Darlington Transistors

Figure shows the direct coupling of two stages of emitter follower amplifier. This cascaded connection of two emitter followers is called the Darlington connection.



Assume that the load resistance R_L is such that R_L hoe < 0.1, therefore we can use approximate analysis method for analyzing second stage.

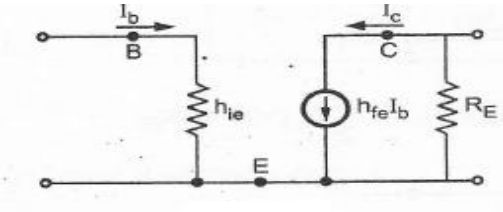
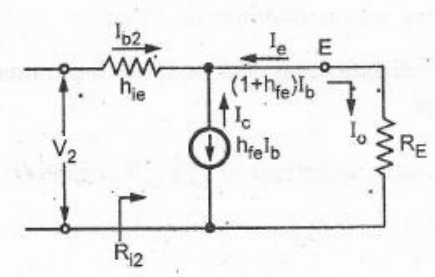


Figure shows approximate h-parameter (AC) equivalent circuit for common emitter configuration. The same circuit can be redrawn by making collector common to have approximate h-parameter equivalent circuit for common collector configuration.



Analysis of second stage :

a) Current Gain (A_{i2}) : $A_{i2} = \frac{I_o}{I_b} = -\frac{I_e}{I_b} = \frac{I_b + h_{fe} I_b}{I_b} = \frac{I_b(1+h_{fe})}{I_b}$

$\therefore$ $\boxed{A_{i2} = 1 + h_{fe}}$

b) Input Resistance (R_{i2}) : $R_{i2} = \frac{V_2}{I_{b2}}$

Applying KVL to outer loop we get,

$V_2 - I_{b2} h_{ie} - I_o R_E = 0$

$\therefore \quad V_2 = I_{b2} h_{ie} + I_o R_E$

$\therefore \quad \frac{V_2}{I_{b2}} = h_{ie} + \frac{I_o}{I_{b2}} R_E$

$\therefore \quad R_{i2} = h_{ie} + A_{i2} R_E \quad$ since, $\frac{I_o}{I_{b2}} = A_{i2}$

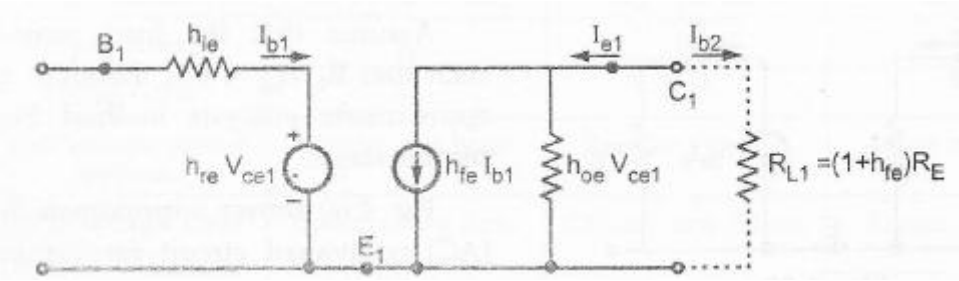
$\therefore \quad \boxed{R_{i2} = h_{ie} + (1 + h_{fe}) R_E}$

$R_{i2} = (1 + h_{fe}) R_E \quad \because h_{ie} << (1 + h_{fe}) R_E$

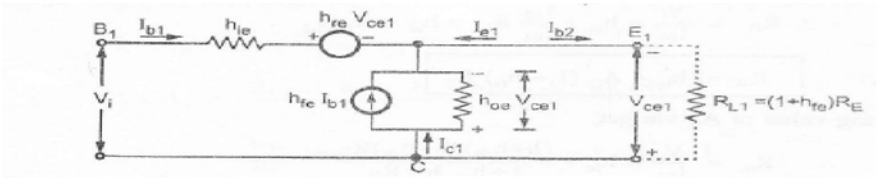
Analysis of first stage :

Load resistance of the first stage is the input resistance of the second stage i.e. R_{i2}. As R_{i2} is high, usually it does not meet the requirement hoe $R_{i2} < 0.1$, and hence we have to use the exact analysis method for analysis of the first stage.

Figure shows the h-parameter equivalent circuit for common emitter configuration.



The same circuit can be redrawn by making collector common to have h-parameter equivalent circuit for common collector for configuration



a) Current Gain (A_{i1}) :

$$A_{i1} = \frac{I_{b2}}{I_{b1}}$$

$$A_{i1} = \frac{I_{e1}}{I_{b1}}$$

$$I_{e1} = -(I_{b1} + I_{c1})$$

and $$I_{c1} = h_{fe}I_{b1} + h_{oe} V_{ce1} = h_{fe}I_{b1} + h_{oe}(-I_{b2} R_{L1}) = h_{fe}I_{b1} + h_{oe} I_{e1} R_{L1}$$

Substituting value of I_{c1} equation we get,

$$\therefore \quad I_{e1} = -(I_{b1} + h_{fe}I_{b1} + h_{oe} I_{e2} R_{L1}) = -I_{b1} - h_{fe}I_{b1} - h_{oe} I_{e1}R_{L1}$$

$$\therefore \quad I_{e1} + h_{oe} R_{L1} I_{e1} = -I_{b1}(1 + h_{fe})$$

$$-\frac{I_{e1}}{I_{b1}} = \frac{1+h_{fe}}{1+h_{oe} R_{L1}}$$

We know that, $R_{L1} = (1 + h_{fe}) R_E$

$$\therefore \quad \boxed{A_{i1} = -\frac{I_{e1}}{I_{b1}} = \frac{1+h_{fe}}{1+h_{oe}(1+h_{fe}) R_E}}$$

$$= \frac{1+h_{fe}}{1+h_{oe} h_{fe} R_E} \quad \because h_{fe} >> 1$$

b) Input Resistance (R_i) : $$R_{i1} = \frac{V_i}{I_{b1}}$$

Applying KVL to output loop we get,

$$V_i - I_{b1} h_{ie} - h_{re} V_{ce1} + V_{ce1} = 0$$

$$\therefore V_i = I_{b1}h_{ie} + h_{re} V_{ce1} - V_{ce1}$$

The terms $h_{re} V_{ce1}$ is negligible since h_{re} is in the order of 2.5×10^{-4}

$$= I_{b1}h_{ie} - (-I_{b2}R_{L1}) = I_{b1}h_{ie} + I_{b2}R_{L1}$$

$$\therefore R_{i1} = \frac{V_i}{I_{b1}} = h_{ie} + \frac{I_{b2}}{I_{b1}} R_{L1} = h_{ie} + A_{i1}R_{L1}$$

$$\therefore \quad \boxed{R_{i1} = h_{ie} + A_{i1}(1 + h_{fe}) R_E}$$

Substituting value of A_{i1} we get,

$$R_{i1} = \frac{V_i}{I_{b1}} = h_{ie} + \frac{(1+h_{fe})(1+h_{fe})R_E}{1+h_{oe}\,h_{fe}\,R_E}$$

$$\therefore \quad \boxed{R_{i1} = h_{ie} + \frac{(1+h_{fe})^2 R_E}{1+h_{oe}\,h_{fe}\,R_E}}$$

$$\therefore \quad \boxed{R_{i1} \approx \frac{(1+h_{fe})^2 R_E}{1+h_{oe}\,h_{fe}\,R_E}} \qquad \because h_{ie} << \frac{(1+h_{fe})^2 R_E}{1+h_{oe}\,h_{fe}\,R_E}$$

Overall current gain(Ai)

$$A_i = A_{i1} \times A_{i2}$$

$$= \frac{1+h_{fe}}{1+h_{oe}\,(1+h_{fe})\,R_E} \times (1 + h_{fe})$$

$$\therefore \quad \boxed{A_i = \frac{(1+h_{fe})^2}{1+h_{oe}\,(1+h_{fe})\,R_E}}$$

From table, we can say that Darlington connection improves input impedance as well as current gain of the circuit

Overall Voltage gain

Parameter	Single stage	Darlington
Input resistance	$R_i = (1 + h_{fe})\,R_E = 168.3\ k\Omega$	$R_i = \frac{(1+h_{fe})^2 R_E}{1+h_{oe}\,(1+h_{fe})\,R_E} \approx 1.65\ M\Omega$
Current gain	$A_i = 1 + h_{fe} = 51$	$A_i = \frac{(1+h_{fe})^2}{1+h_{oe}\,(1+h_{fe})\,R_E} \approx 500$

We know that

$$A_v = \frac{A_i R_L}{R_i}$$

By subtracting 1 on both sides we get

$$1 - A_v = 1 - \frac{A_i R_L}{R_i}$$

$$\therefore \quad 1 - A_v = \frac{R_i - A_i R_L}{R_i} = \frac{h_{ic} + h_{rc} A_i R_i - A_i R_L}{R_i}$$

$$= \frac{h_{ie}}{R_i} \text{ since } h_{ic} = h_{ie} \text{ and } h_{rc} = 1 - h_{re} \approx 1$$

$$\therefore \quad A_v = 1 - \frac{h_{ie}}{R_i}$$

We know that the overall voltage gain in multistage amplifier is a product of individual voltage gain

$$\therefore \quad A_v = A_{v1} A_{v2} = \left(1 - \frac{h_{ie}}{R_{i1}}\right)\left(1 - \frac{h_{ie}}{R_{i2}}\right)$$

$$\therefore \quad \boxed{A_v = 1 - \frac{h_{ie}}{R_{i2}} - \frac{h_{ie}}{R_{i1}} + \frac{h_{ie}^2}{R_{i1} R_{i2}}}$$

As we know, input resistance Ri1 >> Ri2 we can neglect term 3 and term 4 in the above equation.

$$\therefore \quad \boxed{A_v \approx 1 - \frac{h_{ie}}{R_{i2}}}$$

Output Impedance (Ro_2) :

$$R_o = \frac{1}{\text{Output admittance}} = \frac{1}{Y_o}$$

From equation, Yo of the transistor is given as

$$Y_o = Y_{o1} = h_{oc} - \frac{h_{fc} . h_{rc}}{h_{ic} + R_s} = h_{oe} - \frac{-(1 + h_{fe})}{h_{ie} + R_s}$$

Since

$$h_{oc} = h_{oe,}$$

$$h_{fc} = -(1 + h_{fe})$$

And

$$h_{ic} = h_{ie}$$

$$Y_{o1} = h_{oe} + \frac{(1+h_{fe})}{h_{ie}+R_s}$$

$$Y_{o1} = \frac{1+h_{fe}}{h_{ic}+R_s}$$

$$\because \quad h_{oe} << \frac{(1+h_{fe})}{h_{ic}+R_s}$$

$$\therefore \quad R_{o1} = \frac{1}{Y_{o1}}$$

$$\therefore \quad \boxed{R_{o1} = \frac{h_{ie1}+R_s}{1+h_{fe}}}$$

we can see that the R_{i1} of the first stage is the source

Resistance for second stage, i.e. $R_{S2}= R_{O1}$

$$\left(\frac{h_{ie1}+R_s}{\quad}\right)+h_{ie2}$$

Since the current in T_2 is $1+h_{fe}$ times the current in T_1, $h_{ie1} \approx (1+h_{fe})h_{ie2}$ substituting this value of h_{ie1} in equation 15 we get,

$$R_{o2} = \frac{(1+h_{fe})h_{ie2}+R_s}{(1+h_{fe})^2} + \frac{h_{ie2}}{1+h_{fe}} = \frac{h_{ie2}}{1+h_{fe}} + \frac{R_s}{(1+h_{fe})^2} + \frac{h_{ie2}}{1+h_{fe}}$$

$$\therefore \quad \boxed{R_{o2} = \frac{R_s}{(1+h_{fe})^2} + \frac{2h_{ie2}}{(1+h_{fe})}}$$

Key Point:

- In above analysis we have assumed that the h-parameter of T1 and T2 are identical,
- From the above analysis we have seen that Darlington connection of two transistors improves current gain and input resistance of the circuit.

16. Explain about Bootstrap Emitter Follower technique.[CO2-H2]

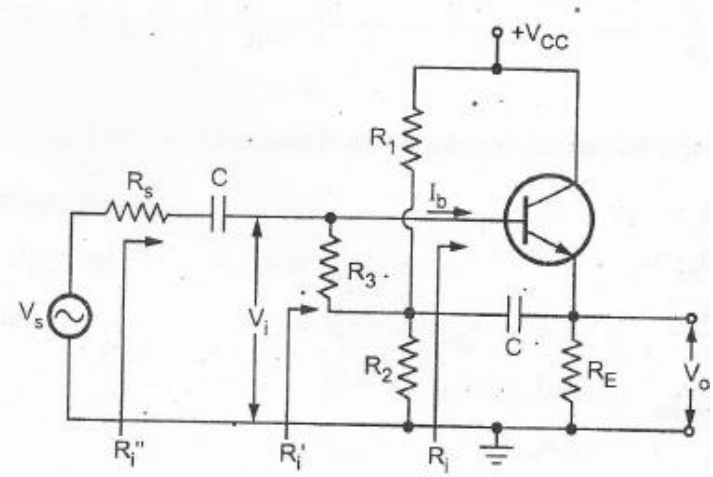


Fig. Bootstrap emitter follower

In emitter follower, the input resistance of the amplifier is reduced because of the shunting effect of the biasing resistors. To overcome this problem the emitter follower circuit is modified, as shown in the Figure. Here, two additional components are used, resistance R, and capacitor C .The capacitor, is connected between the emitter and the junction of R1,R2 and R3.

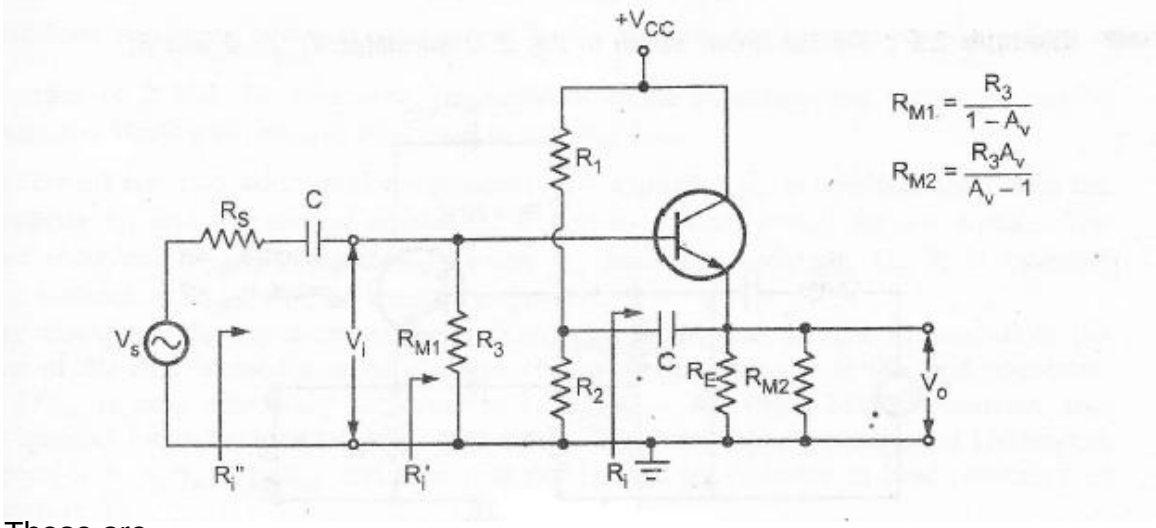
For d.c. signal, capacitor C acts as a open circuit and therefore resistance R1,R2 and R3 provides necessary biasing to keep the transistor in active region.

For ac signal, the capacitor acts as a short circuit. Its value is chosen such that it provides very low reactance nearly short circuit at lowest operating frequency. Hence for ac, the bottom of R3 is effectively connected to the output(the emitter), whereas the top of R3 is at the -input. (the base). In other words, R3 is connected between input node and output node. For such connection effective input resistance is given by Miller's theorem.

The two components are

$$\frac{Z}{1-K} \quad \text{and} \quad \frac{Z \cdot K}{K-1}$$

R3 is the impedance between output voltage and input voltage and K is the voltage gain.



These are

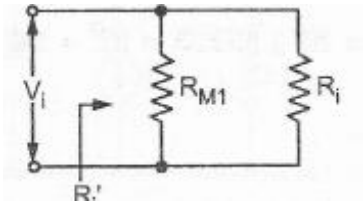
$$R_{M1} = \frac{R_3}{1-A_v} \text{ and } R_{M2} = \frac{R_3 A_v}{A_v - 1}$$

Since, for an emitter follower, Av, approaches unity, then R_{M2} becomes extremely large.

$$R_i' = R_i \parallel R_M$$

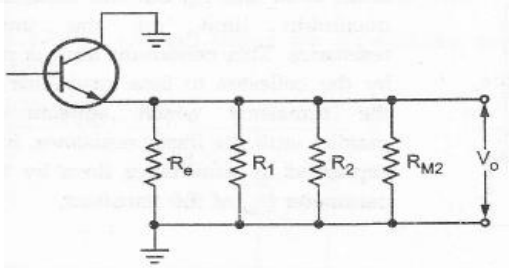
$$R_i = h_{ie} + (1 + h_{fe}) R_E$$

The above effect, when Av tends to unity is called bootstrapping. The name arises from the fact that, if one end of the resistor R_3 changes in voltage, the other end of R_3 moves through the same potential difference; it is as if R_3 is pulling itself up by its bootstraps.



The effective load on the emitter follower can be given as

$$R_{L\,eff} = R_E \parallel R_1 \parallel R_2 \parallel R_{M2}$$



Because of the capacitor, biasing resistances R1 and R2, come on output side shunting effective load resistance. The resistance R_{M2} is very large and hence it is often neglected.

$$\therefore \quad R_{L\,eff} = R_E \parallel R_1 \parallel R_2$$

Unit-III

JFET and MOSFET Amplifiers

Part- A

1. Define JFET Amplifier? [CO3-L1]

It provides an excellent voltage gain with high input impedance. Due to these characteristics, it is often preferred over BJT. Three basic FET configurations Common source, common drain and common gate

2. Draw the JFET low frequency AC Equivalent circuit. [CO3-L2]

Figure shows the small signal low frequency a.c Equivalent circuit for n-channel JFET.

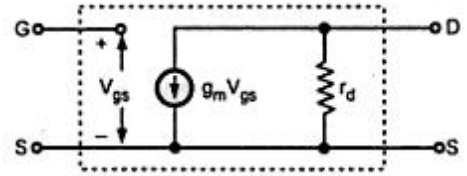


Fig3.1 small signal model of JFET

3. Common Source Amplifier With Fixed Bias [CO3-L2]

Figure shows Common Source Amplifier with Fixed Bias. The coupling capacitor C1 and C2 which are used to isolate the dc biasing from the applied ac signal act as short circuits for ac analysis.

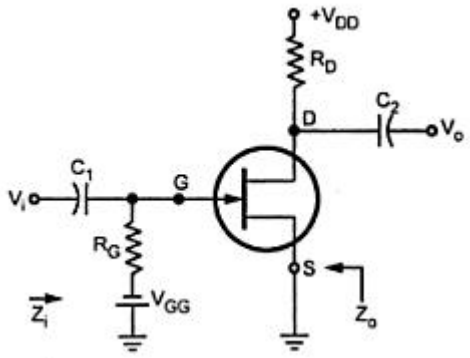


Fig3.2 Common source circuit of JFET

4. what is the Need for Cascading in amplifier stages? [CO3-L1]

For faithful amplification amplifier should have desired voltage gain, current gain and it should match its input impedance with the source and output impedance with the load. In such situations more than one amplifier stages are cascaded such that input and output stages provide impedance matching requirements.

5. Define voltage gain? [CO3-L1]

It is given by

$$A_v = \frac{V_o}{V_i}$$

6. Why the electrolytic capacitor is not used for coupling? [CO3-L2]

Electrolytic capacitor is a polarized capacitor. So it cannot be used for coupling and also in electrolytic capacitor, the dielectric is not an insulating material but it conducting material which will change the capacitance effect.

7. Write a note on effects of coupling capacitor. [CO3-L1]

The coupling capacitor Co transmits AC Signal. But blocks Dc. This prevents DC interferences between various stages and the shifting of operating point.
It prevents the loading effect between adjacent stages.

8. What is the significance of gain bandwidth product? [CO3-L2]

It is very helpful in the preliminary design of a multistage wideband amplifier. This can be used to setup a tentative circuit, which is often used for this purpose.

9. Why N-channel FET's have a better response than P-channel FET's? [CO3-L1]

N- channel FET have a better high frequency response than P-channel FET due to the following reason. Mobility of electrons is large in N-channel FET whereas the mobility of holes is poor in P-channel FET. The input noise is less in N-channel FET that that of the P-channel FET. The trains conductance is larger in N-channel FET that that of P-channel Fet.

10. Define Miller effect in input capacitance? [CO3-L2]

For any inverting amplifier, the input capacitance will be increased by a miller effect capacitance, sensitive to the gain of the amplifier and the inter electrode capacitance connected between the input and output terminals of the active device.

$$CMi = (1-Av)\,Cf \; ; \; CMo = Cf$$

Cf = Inter electrode capacitance between input and output.

11. What is a Darlington connection in the amplifiers? [CO3-L2]

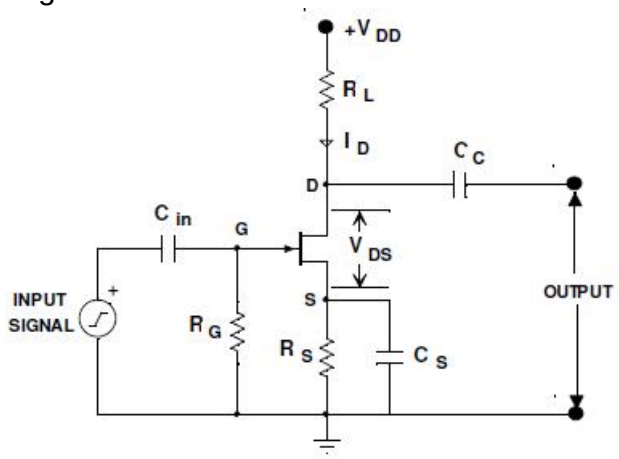
A Darlington transistor connection provides a transistor having a very large current gain, typically a few thousand. The main features of the Darlington connection is that the composite transistor acts as a single unit with a current gain, that is the product of current gains of the individual transistors.

12. Give the Applications of JFET [CO3-L3]

FET is used as a
(1) Buffer amplifier (2) Low Noise Amplifier (3) Cascaded Amplifier (4) Analog Switch (5) Chopper (6) Phase Shift Oscillator circuits (7) Voltage Variable Resistors in Operational Amplifiers and tone controls etc., (8) For Mixer operation on FM and TV receivers

13. **Draw a single stage amplifier circuit using JFET [CO3-L2]**

The circuit of a Single Stage Common Source N-channel JFET amplifier using self bias is shown in fig



14. What is the purpose of input capacitor, Cin in single stage common source JFET amplifier? [CO3-L3]

An ac signal is supplied to the gate of the FET through an electrolytic capacitor called input capacitor Cin. This capacitor allows only ac signal enter the gate but isolates the signal source from RG. If this capacitor is not used, the signal source resistance will come across the resistor RG and thus changing the biasing conditions.

15. What is the purpose of Biasing Network (Rs and Cs) in single stage common source JFET amplifier? [CO3-L2]

The JFET is self-biased by using the biasing network Rs- Cs. The desired bias voltage is obtained when dc component of drain current flows through the source-biasing resistor Rs. whereas, the capacitor Cs bypasses the ac component of drain current.

16. What is the purpose of Coupling Capacitor (Cc) in single stage common source JFET amplifier? [CO3-L1]

It is an electrolytic capacitor used to couple one stage of amplification to the next stage or load. It allows only amplified ac signal to pass to the other side but blocks the dc voltage. If this capacitor is not used, the biasing conditions of the next stage will be drastically changed due to the shunting effect of Rd.

17. Give the expression for I_D for E-MOSFET. [CO3-L3]

$$I_D = (K(V_{GS} - V_T)2$$

PART B

1. Explain about Common Source, common collector, common emitter Amplifier with Fixed Bias [CO3-H2]

Figure shows Common Source Amplifier with Fixed Bias. The coupling capacitor C1 and C2 which are used to isolate the dc biasing from the applied ac signal act as short circuits for ac analysis.

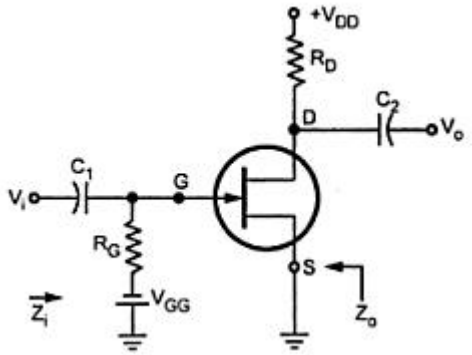


Fig3.2 Common source circuit of JFET

The following figure shows the low frequency equivalent model for Common Source Amplifier With Fixed Bias. It is drawn by replacing

- All capacitors and dc supply voltages with short circuit
- JFET with its low frequency a.c Equivalent circuit

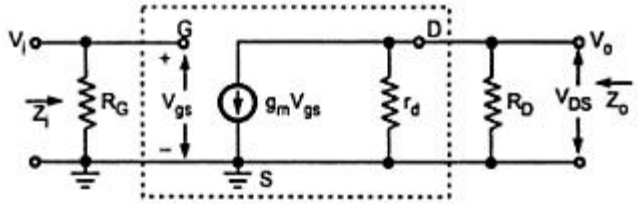


Fig3.3 small signal model of CS JFET amplifier

Input Impedance Zi

$Zi = R_G$

Output Impedance Zo

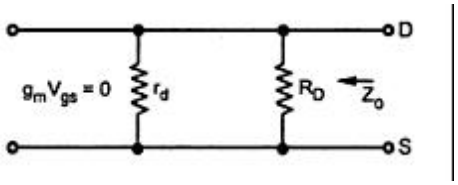


Fig3.4 Equivalent circuit model of JFET for output

It is the impedance measured looking from the output side with input voltage Vi equal to Zero. As Vi=0,Vgs =0 and hence g_mVgs =0 . And it allows current source to be replaced by an open circuit.

So,

$$Z_o = R_D \,||\, r_d$$

If the resistance rd is sufficiently large compared to R_D, then

$$Z_o \approx R_D \qquad \because r_d >> R_D$$

Voltage Gain A_v :

The voltage gain $A_v = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i}$

Looking at Fig. we can write

$$V_o = -g_m V_{gs} \; (r_d \,||\, R_D)$$

As we know $V_i = V_{gs}$ we can write

$$V_o = -g_m V_i \; (r_d \,||\, R_D)$$

$$\therefore \quad A_v = \frac{V_o}{V_i} = -g_m \; (r_d \,||\, R_D)$$

and if $r_d >> R_D$,

$$A_v \approx -g_m R_D$$

Table summarizes performance of common source amplifier with fixed bias.

Parameter	Exact	With $r_d >> R_D$
Z_i	R_G	R_G
Z_o	$R_D \| r_d$	R_D
A_v	$-g_m \; (R_D \,\|\|\, r_d)$	$-g_m R_D$

Common source amplifier with self bias (Bypassed Rs)

Figure shows Common Source Amplifier With self Bias. The coupling capacitor C1 and C2 which are used to isolate the d.c biasing from the applied ac signal act as short circuits for ac analysis. Bypass capacitor Cs also acts as a short circuits for low

frequency analysis.

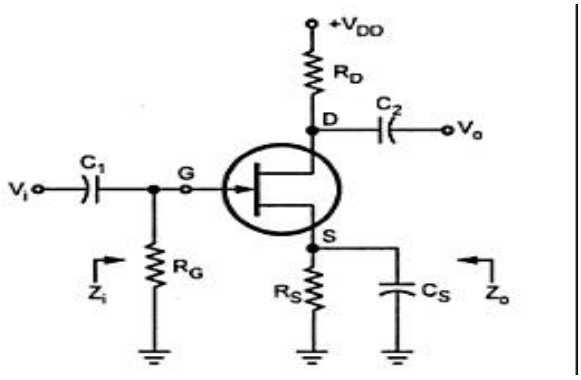


Fig3.5 **Common source amplifier model of JFET**

The following figure shows the low frequency equivalent model for Common Source Amplifier With self Bias.

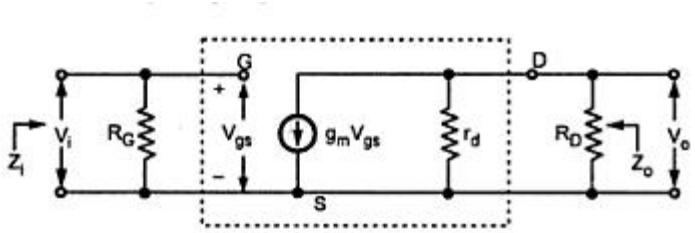


Fig3.6 **Small signal model for Common source amplifier** model of JFET

i) Input impedance Z_i :	$Z_i = R_G$
ii) Output impedance Z_o :	$Z_o = r_d \,\|\|\, R_D$
if $r_d >> R_D$	$Z_o \approx R_D$
iii) Voltage gain A_v :	$A_v = -g_m (r_d \,\|\|\, R_D)$
If $r_d >> R_D$	$A_v = -g_m R_D$

The negative sign in the voltage gain indicates there is a 180^o phase shift between input and output voltages.

Common source amplifier with self bias (un bypassed Rs)

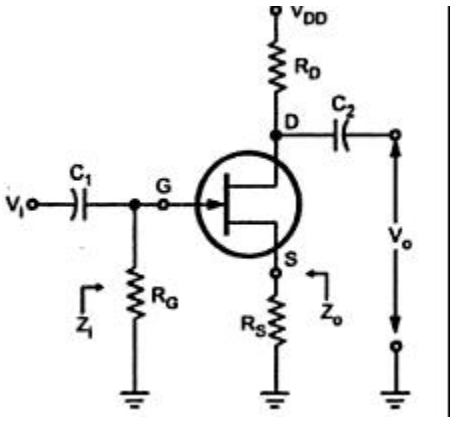


Fig3.7 **Common source amplifier** model of JFET

Now Rs will be the part of low frequency equivalent model as shown in figure.

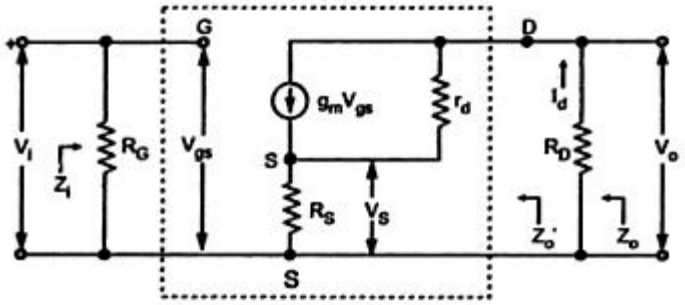


Fig3.8 **Small signal model for Common source amplifier** model of JFET

Input Impedance Zi

$Zi = R_G$

Output Impedance Zo

It is given by

$$Z_o = Z_o' \| R_D$$

where $$Z_o' = \left.\frac{V_o}{I_d}\right|_{V_i = 0}$$

$$Z_o = [\, r_d + R_s (\mu + 1) \,] \| R_D$$

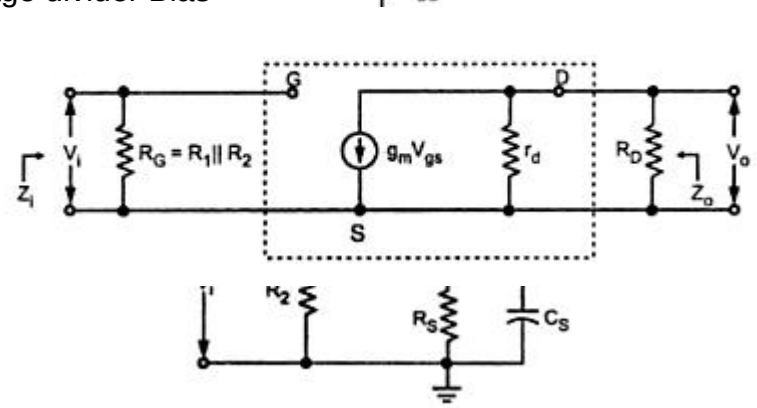
$$Z_o = [\, r_d + R_s (g_m r_d + 1) \,] \| R_D$$

Common source amplifier with Voltage divider bias (Bypassed Rs)

Figure shows Common Source Amplifier With voltage divider Bias. The coupling capacitor C1 and C2 which are used to isolate the d.c biasing from the applied ac signal act as short circuits for ac analysis. Bypass capacitor Cs also acts as a short circuits for low frequency analysis.

Common source amplifier with Voltage divider bias(Bypassed Rs)

The following figure shows the low frequency equivalent model for Common Source Amplifier With voltage divider Bias



small model of Common source amplifier with Voltage divider bias(Bypassed Rs)

The parameters are given by

$$R_G = R_1 \,||\, R_2$$

$$Z_i = R_G = R_1 \,||\, R_2$$

$$Z_o = r_d \,||\, R_D$$

if $r_d >> R_D$

$$Z_o \approx R_D$$

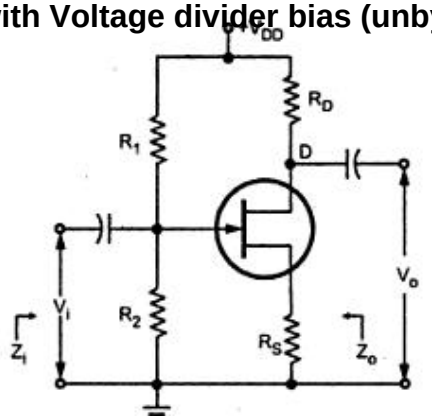
$$A_v = -g_m (r_d \,||\, R_D)$$

If $r_d >> R_D$

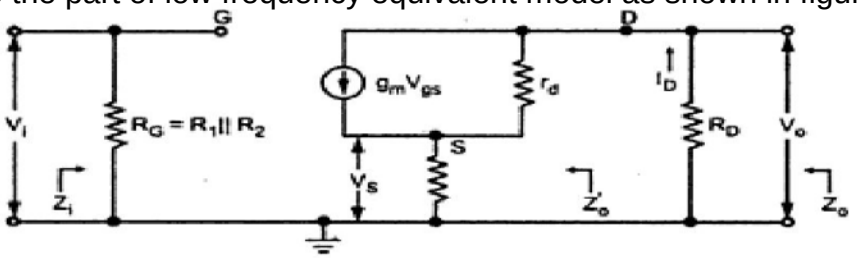
$$A_v = -g_m R_D$$

The negative sign in the voltage gain indicates there is a 180^o phase shift between input and output voltages.

Common source amplifier with Voltage divider bias (unbypassed Rs)



Now Rs will be the part of low frequency equivalent model as shown in figure.



It is important to note that, here, $R_G = R_1 \| R_2$.

$$Z_i = R_G = R_1 \| R_2$$

$$Z_o' = r_d + g_m R_s r_d + R_s$$

or

$$Z_o' = r_d + R_s (\mu + 1)$$

$$Z_o = [\, r_d + g_m R_s r_d + R_s \,] \| R_D$$

or

$$Z_o = [\, r_d + R_s (\mu + 1) \,] \| R_D$$

$$A_v = \frac{-g_m R_D}{1 + g_m R_s + \frac{R_s + R_D}{r_d}}$$

Common Drain Amplifier

In this circuit, input is applied between gate and source and output is taken between source and drain.

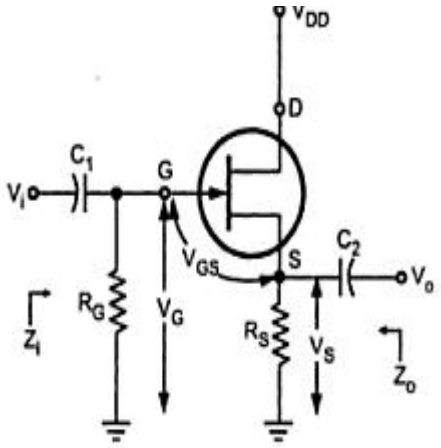


Fig3.12 **Circuit of Common Drain amplifier**

In this circuit, the source voltage is

$$Vs = V_G + V_{GS}$$

When a signal is applied to the JFET gate via C1 ,VG varies with the signal. As VGS is fairly constant and $Vs = V_G + V_{GS}$, Vs varies with Vi.

The following figure shows the low frequency equivalent model for common drain circuit.

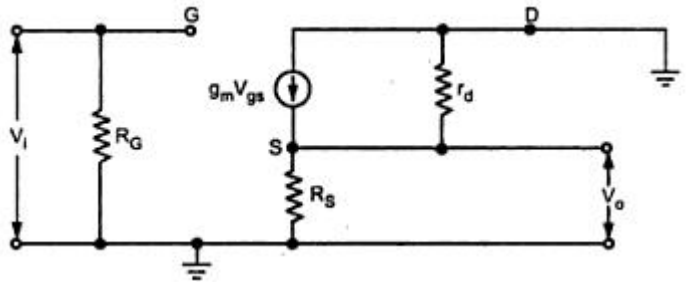


Fig **small model of Common Drain amplifier**

Input Impedance Zi

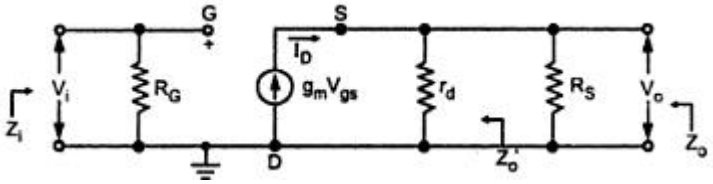


Fig Simplified small model of Common Drain amplifier

$Zi = R_G$

Output Impedance Zo

It is given by

$$Z_o = Z_o' || R_s$$

where $$Z_o' = \left.\frac{V_o}{I_d}\right|_{V_i = 0}$$

Applying KVL to the outer loop we can have,

$$V_i + V_{gs} - V_o = 0$$

As $$V_i = 0,$$

$$V_{gs} = V_o$$

Looking at Fig. we can write that,

$$g_m V_{gs} = I_d$$

But Vgs = Vo, so

$$g_m V_o = I_d$$

$$Z_o' = \frac{V_o}{I_d} = \frac{1}{g_m}$$

$$\therefore \quad Z_o = \frac{1}{g_m} || R_s$$

Voltage gain (Av)

It is given by

$$A_v = \frac{V_o}{V_i}$$

Looking at Fig. we can write that,

$$V_o = -I_d (r_d \,||\, R_s)$$

and $$I_d = g_m V_{gs}$$

$$\therefore \quad V_o = -g_m V_{gs} (r_d \,||\, R_s)$$

But

$$V_i = -V_{gs} + V_o$$
$$= -V_{gs} + [-g_m V_{gs} (r_d \,||\, R_s)]$$

Substitute the value Vo and Vi. Then

$$A_v = \frac{-g_m V_{gs} (r_d \,||\, R_s)}{-V_{gs} (1 + g_m (r_d \,||\, R_s))}$$

$$= \frac{g_m (r_d \,||\, R_s)}{1 + g_m (r_d \,||\, R_s)}$$

if $r_d >> R_s$

$$A_v = \frac{g_m R_s}{1 + g_m R_s}$$

if $g_m R_s >> 1$

$A_v \approx 1$, but it is always less than one.

Common drain circuit does not provide voltage gain.& there is no phase shift between input and output voltages.

Table summarizes the performance of common drain amplifier

	Exact	$r_d >> R_D$
Z_i	R_G	R_G
Z_o	$\frac{1}{g_m} \,\|\|\, R_s$	$\frac{1}{g_m} \,\|\|\, R_s$
A_v	$\frac{g_m (r_d \,\|\| R_s)}{1 + g_m (r_d \,\|\| R_s)}$	$\frac{g_m R_s}{1 + g_m R_s}$

Common Gate Amplifier

In this circuit, input is applied between source and gate and output is taken between drain and gate.

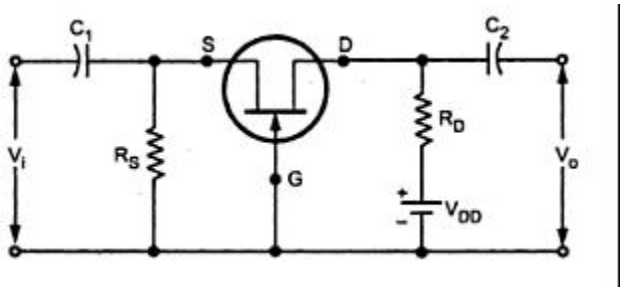


Fig3.14 **Circuit diagram of Common gate amplifier**

In CG Configuration, gate potential is at constant potential. so, increase in input voltage Vi in positive direction increase the negative gate source voltage. Due to I_D reduces, reduces, reducing the drop I_DR_D. Since $V_D= V_{DD}-I_DR_D$, the reduction in I_D results in an increase in output voltage.

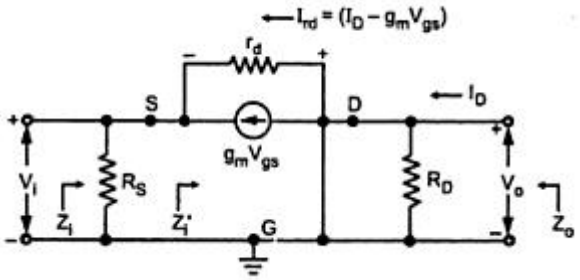


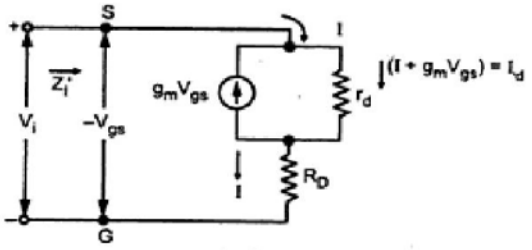
Fig3.15 **small signal model for Common gate amplifier**

1. Input Impedance (Zi)

It is given by

$$Z_i' = \frac{V_i}{I}$$

And



$$I_{rd} = I + g_m V_{gs}$$

$$\therefore \quad I = I_{rd}\ g_m V_{gs}$$

where $$I_{rd} = \frac{V_i - IR_D}{r_d}$$

After substituting and simplification,

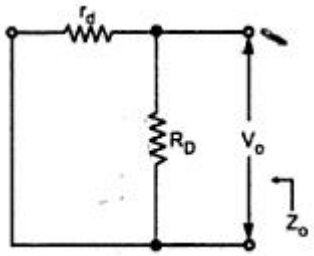
$$\frac{V_i}{I} = \frac{1+\frac{R_D}{r_d}}{\frac{1}{r_d}+g_m} = \frac{r_d + R_D}{1+g_m r_d}$$

And

If $r_d >> R_D$ and $g_m r_d >> 1$ then we can write,

$$Z_i = R_s \parallel \frac{r_d}{g_m r_d} = R_s \parallel \frac{1}{g_m}$$

2. Output Impedance Zo



It is given by

$$Z_o = r_d \parallel R_D$$

If $r_d >> R_D$

$$Z_o \approx R_D$$

3. Voltage gain (Av)

It is given by

$$A_v = \frac{V_o}{V_i}$$

$$V_o = -I_D R_D$$

$$V_i = -V_{gs}$$

Using KVL to the outer loop, after simplification

$$A_v = \frac{V_o}{V_i} = \frac{-I_d + R_D}{\dfrac{-I_d(r_d + R_D)}{1 + g_m r_d}}$$

$$= \frac{R_D(1 + g_m r_d)}{r_d + R_D}$$

If $r_d >> R_D$ and $g_m r_d >> 1$

$$A_v = \frac{R_D(g_m r_d)}{r_d} = R_D g_m$$

Table summarizes the performance of common gate amplifier

	Exact	$r_d >> R_{OD}$
Z_i	$R_s \parallel \left[\frac{r_d + R_D}{1 + g_m r_d}\right]$	$R_s \parallel \frac{1}{g_m}$
Z_o	$r_d \parallel R_D$	R_D
A_v	$\frac{R_D(1 + g_m r_d)}{r_d + R_D}$	$g_m R_D$

2. Explain the Multistage Amplifier and its characteristics. [CO3-H2]

In practice, we need amplifier which can amplify a signal from a very weak source such as a microphone, to a level which is suitable for the operation of another transducer such as loudspeaker . This is achieved by cascading number of amplifier stages, known as multistage amplifier

1. Need for Cascading

For faithful amplification amplifier should have desired voltage gain, current gain and it should match its input impedance with the source and output impedance with the load. Many times these primary requirements of the amplifier cannot be achieved with single stage amplifier, because of the limitation of the transistor/FET parameters. In such situations more than one amplifier stages are cascaded such that input and output stages provide impedance matching requirements with some amplification and remaining middle stages provide most of the amplification.

We can say that,

- When the amplification of a single stage amplifier is not sufficient, or,
- When the input or output impedance is not of the correct magnitude, for a particular application two or more amplifier stages are connected, in cascade. Such amplifier, with two or more stages is also known as multistage amplifier.

2. Two Stage Cascaded Amplifier

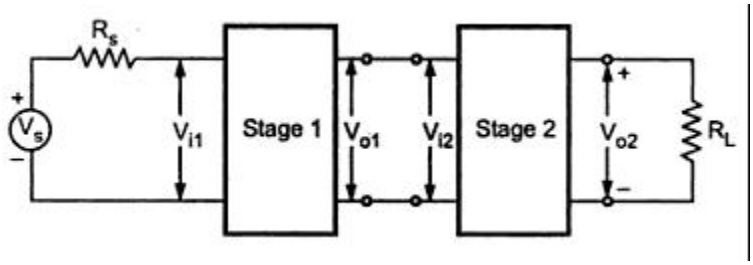
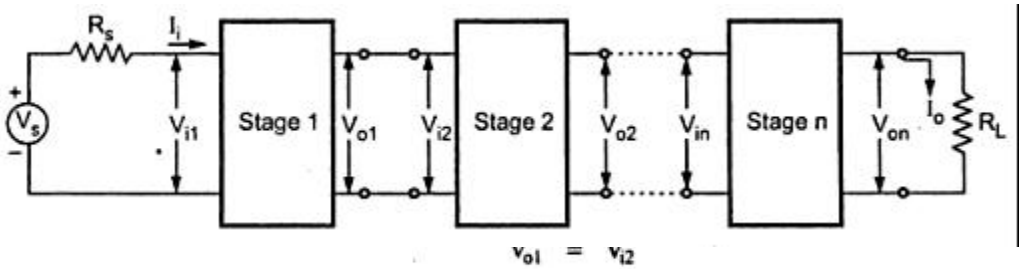


Fig **Cascaded amplifier**

Vi1 is the input of the first stage and Vo2 is the output of second stage. So,Vo2/Vi1 is the overall voltage gain of two stage amplifier.

3. n-Stage Cascaded Amplifier



$$v_{o1} = v_{i2}$$

$$\therefore A_V = \frac{V_{o2}}{V_{i2}} \frac{V_{o1}}{V_{i1}}$$

$$= A_{V2} A_{V1}$$

Fig3.17 Multistage **amplifier**

Voltage gain :

The resultant voltage gain of the multistage amplifier is the product of voltage gains of the various stages.

Av = Avl Av2 ... Avn

Gain in Decibels

In many situations it is found very convenient to compare two powers on logarithmic scale rather than on a linear scale. The unit of this logarithmic scale is called decibel (abbreviated dB). The number N decibels by which a power P2 exceeds the power P1 is defined by

$$N = 10 \log \frac{P_2}{P_1}$$

Decibel, dB denotes power ratio. Negative values of number of dB means that the power P2 is less than the reference power P1 and positive value of number of dB

means the power P2 is greater than the reference power P1.

For an amplifier, P1 may represent input power, and P2 may represent output power. Both can be given as

$$P_1 = \frac{V_i^2}{R_i} \text{ and } P_2 = \frac{V_o^2}{R_o}$$

Where Ri and Ro are the input and output impedances of the amplifier respectively.Then,

$$N = 10 \log_{10} \frac{V_o^2 / R_o}{V_i^2 / R_i}$$

If the input and output impedances of the amplifier are equal i.e. Ri = Ro= R, then

$$N = 10 \log_{10} \frac{V_o^2}{V_i^2} = 10 \log_{10} \left(\frac{V_o^2}{V_i^2} \right) = 10 \times 2 \log_{10} \frac{V_o}{V_i} = 20 \log_{10} \frac{V_o}{V_i}$$

4. Gain of Multistage Amplifier in dB

The gain of a multistage amplifier can be easily calculated if the gain of the individual stages are known in dB, as shown below

$20 \log_{10} Av = 20 \log_{10} Avl + 20 \log_{10} Av2 + \ldots + 20 \log_{10} Avn$

Thus, the overall voltage gain in dB of a multistage amplifier is the decibel voltage gains of the individual stages. It can be given as

AvdB = AvldB + Av2dB + ... + AvndB

Advantages of Representation of Gain in Decibels

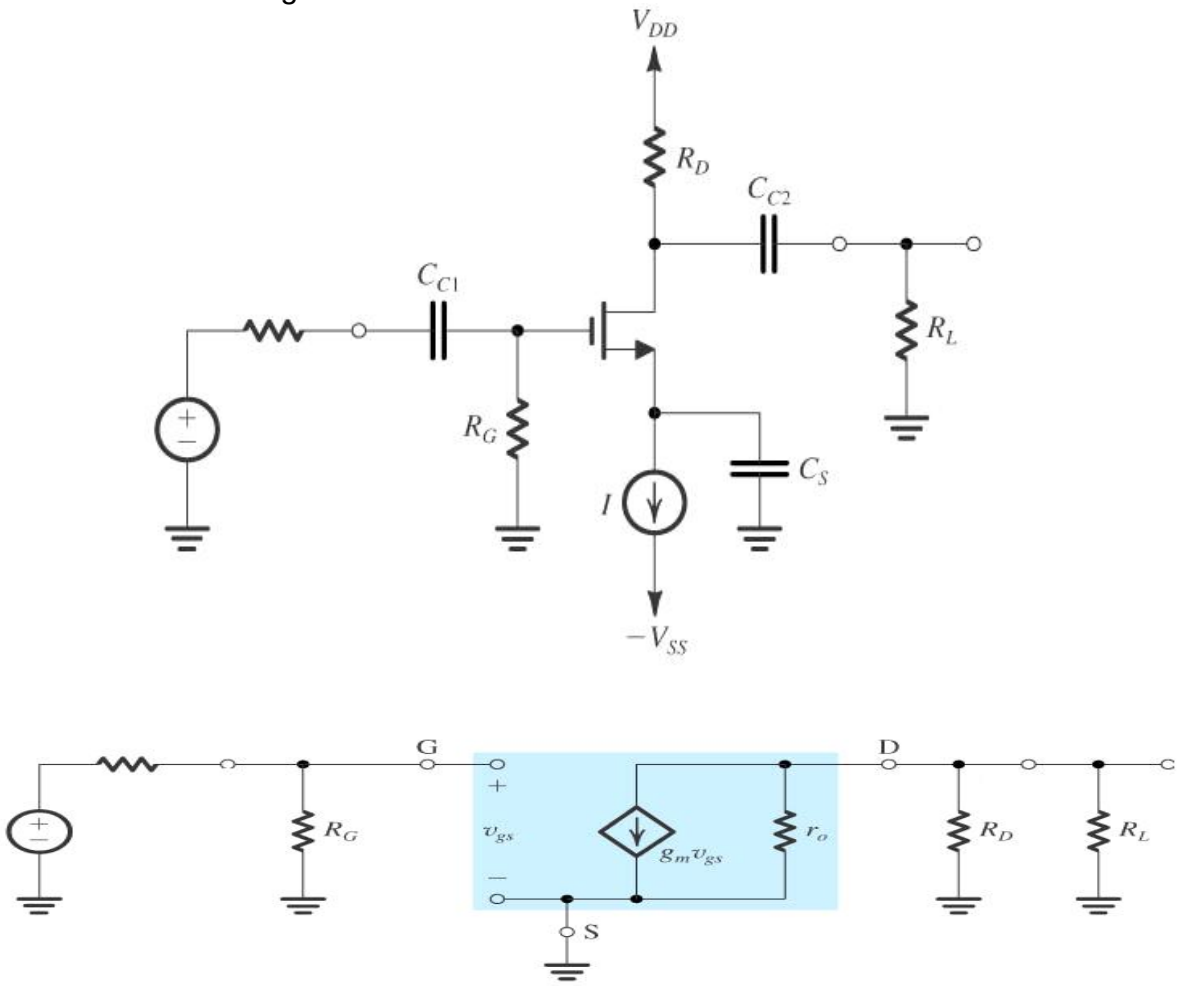
Logarithmic scale is preferred over linear scale to represent voltage and power gains because of the following reasons :

- In multistage amplifiers, it permits to add individual gains of the stages to calculate overall gain.
- It allows us to denote, both very small as well as very large quantities of linear, scale by considerably small figures.

  For example, voltage gain of 0.0000001 can be represented as -140 dB and voltage gain of 1,00,000 can be represented as 100 dB.
- Many times output of the amplifier is fed to loudspeakers to produce sound which is received by the human ear. It is important to note that the ear responds to the sound intensities on a proportional or logarithmic scale rather than linear scale. Thus use of dB unit is more appropriate for representation of amplifier gains.
-

3. Briefly explain about the Small signal Analysis of MOSFET? [CO3-H3]

Common-Source Configuration



$$R_{in} = R_G$$

$$R_o = r_o \,//\, R_D$$

$$A_{vo} = -g_m \cdot (r_o \,//\, R_D)$$

This configuration serves as the gain stage. The disadvantage is high output impedance. Capacitor *CS* is included such that the stage is connected to a current source for biasing

Common-Gate Configuration

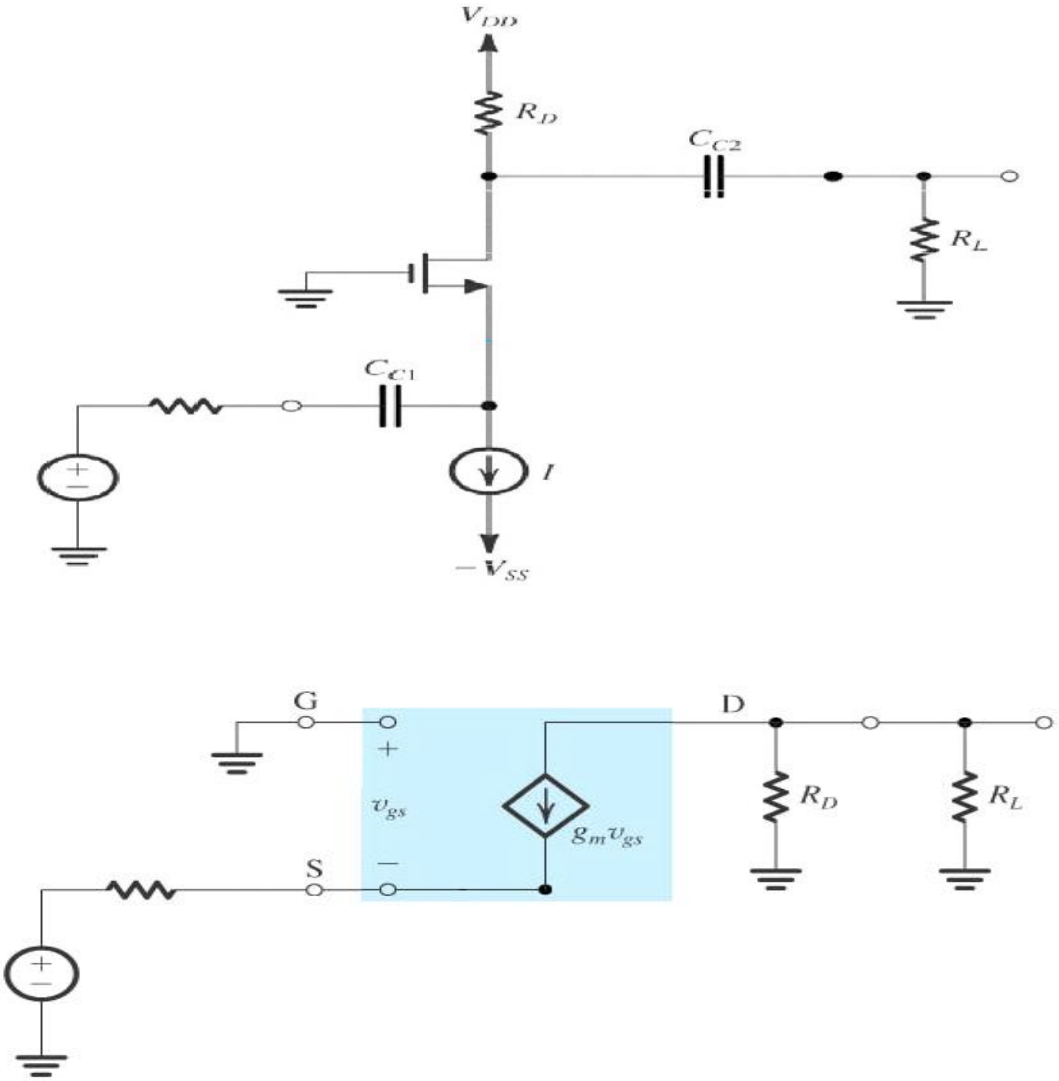


Fig3.18 small signal model of ***Common-gate Configuration of MOSFET***

$$R_{in} = \frac{1}{g_m}$$

$$R_o = R_D$$

$$A_{vo} - g_m \cdot R_D$$

This amplifier provides gain and is useful when a specific (low) *Rin* is required. This is, e.g., the case when the impedance needs to be matched, as with transmission lines (e.g. to 50 Ω). Another application of the CG configuration is that it acts as a current buffer (current gain close to unity, small *Rin*, large *Rout*).

Source Follower (Common-Drain Configuration)

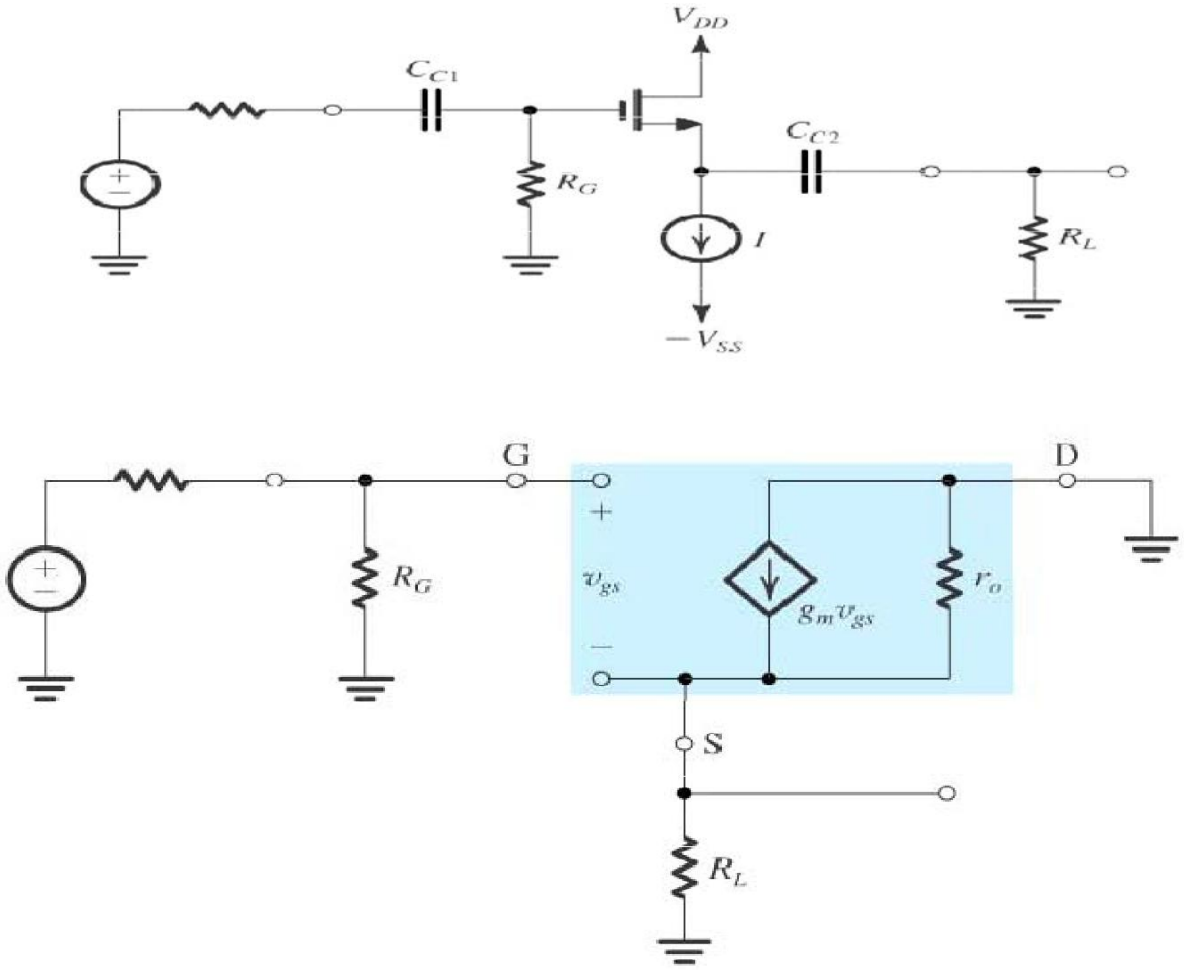


Fig3.20 small signal model of ***Common-drain Configuration of MOSFET***

$$R_{in} = R_G$$

$$R_o = r_o // \frac{1}{g_m} \approx \frac{1}{g_m}$$

$$A_{vo} = \frac{g_m \cdot r_o}{1 + g_m \cdot r_o}$$

This configuration acts as a voltage buffer. It provides no gain, but has low output impedance. It is typically the last stage in a multi-stage amplifier.

4. Explain graphically about the Cascaded Amplifier circuit. [CO3-H3]

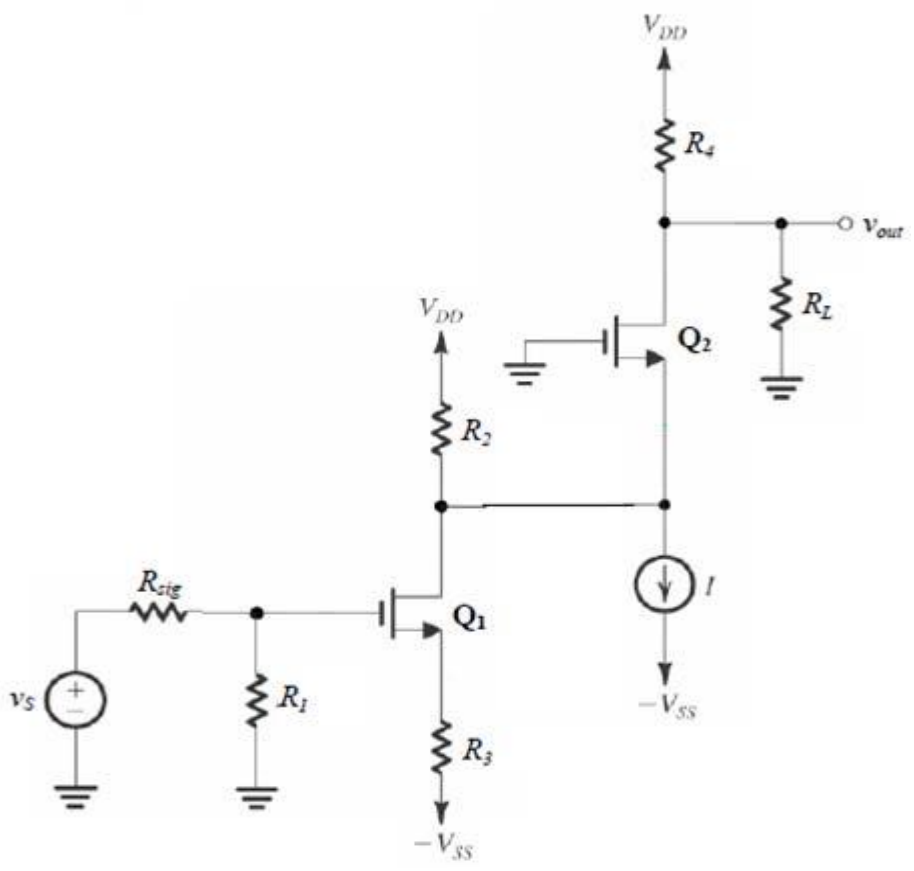
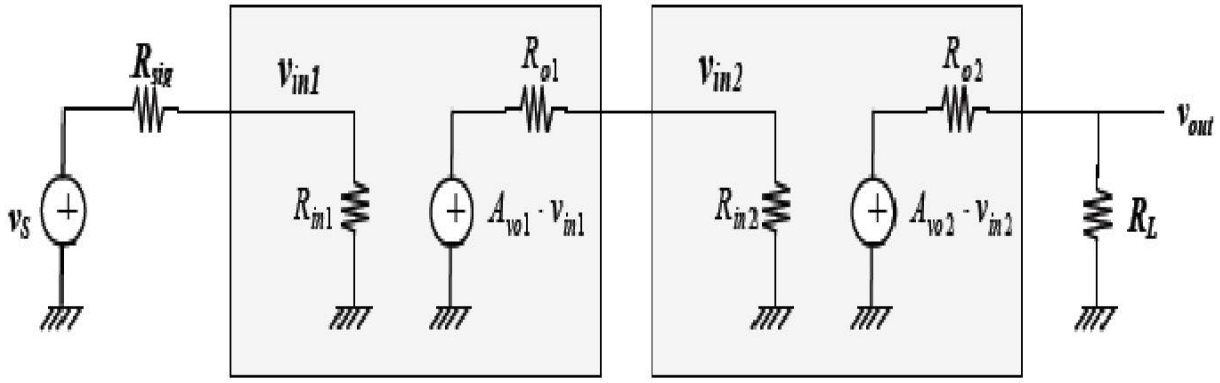


Fig3.21 Cascaded amplifier ***Configuration of MOSFET***Fig3.20 small signal model of Cascaded ***Configuration of MOSFET***



$$A_{vo1} = -\frac{g_{m1} \cdot R_2}{1 + g_{m1} \cdot R_3}$$

$$A_{vo2} = g_{m2} \cdot R_4$$

$$R_{o1} = R_2$$

$$R_{o2} = R_4$$

$$R_{in1} = R_1$$

$$R_{in2} = \frac{1}{g_{m2}}$$

By grouping the different factors in this expression, we can find a physical interpretation for the cascading. This physical interpretation can be used to guide simulation or analysis of the different stages separately, before combining them into a cascaded amplifier.

$$\frac{v_{out}}{v_S} = \frac{v_1}{v_S} \cdot \frac{v_{out}}{v_2} = \underbrace{\left[\frac{R_{in1}}{R_{in1} + R_S} \cdot A_{vo1} \cdot \frac{R_{in2}}{R_{in2} + R_{o1}}\right]}_{\text{Gain of stage 1 with actual source and loaded by stage 2}} \cdot \underbrace{\left[A_{vo2} \cdot \frac{R_L}{R_L + R_{o2}}\right]}_{\text{Gain of stage 2 with ideal source and loaded by } R_L}$$

UNIT –IV

Frequency Analysis of BJTand MOSFET Amplifiers

PART-A

1) **What is the value of relationship between bandwidth and rise time? [CO4-L3]**

$$BW=0.35/t_r$$

2) **What does rise time indicate? How it related to upper 3 dB frequency? [CO4-L3]**

The rise time is an indication of how fast the amplifier can respond to a discontinuity in the input voltage.

$f_H = 0.35/t_r$

3) **What are the high frequency effects ? [CO4-L1]**

At high frequencies, the coupling and bypass capacitor act as a short circuit and do not affect the amplifier frequency response. However, at high frequencies , the internal capacitance, commonly known as junction capacitances do come into play, reducing the circuit gain.

At high frequencies , the reactance of the junction capacitances are low. As frequency increases , the reactance of the junction capacitances fall. When these effect as they are in parallel with junctions. This reduces the circuit gain and hence the output voltage.

4) **If the rise time of a BJT is 35ns, what is the bandwidth that can be obtained using this BJT ? [CO4-L2]**

$t_r=0.35/f_2=0.35/BW$

$BW=0.35/t_r=0.35/35*10^{-9}=10MHz$

5) **Define f_T in a high frequency transistor? [CO4-L1]**

The f_T is the frequency at which short circuit CE current gain becomes unity.

6) **Define rise time? [CO4-L2]**

The rise time is the time required for a signal to change from 10% value to a 90% of its value.

7) **Define sag in an amplifier? [CO4-L1]**

Due to lack of low frequency response the amplifier's output decreases with large time constant. such effect is known as sag.

8) What is bandwidth of an amplifier? [CO4-L2]

The bandwidth of an amplifier is defined as the difference between upper cut-off frequency and the lower cut-off frequency.BW=f_2-f_1

9) If the rise time of a BJT is 40nanoseconds , what is the bandwidth that can be obtained using this BJT ? [CO4-L1]

t_r=0.35/f_2=0.35 /BW

BW=0.35/t_r=0.35/40*10^{-9}

=8.75MHz

10) What is the relation between bandwidth and rise time? [CO4-L1]

We can relate bandwidth with rise time as follows,

BW=f_H=0.35/t_r

11) What is the significance of octaves and decades in frequency response? [CO4-L2]

The octaves and decades are the measure of change in frequency .A ten times change in frequency is called decades. On the other hand, an octave corresponds to doubling or halving of the frequency.

12) Give equation of overall lower and upper frequency of Multistage amplifier? [CO4-L2]

$f_L(n)=f_L/\sqrt{2^{1/n}}-1$

where, $f_L(n)$=Lower 3 db frequency of identical cascaded stages

f_L =Lower 3 db frequency of single stage

n=Number of stages

$f_H(n)=f_H*\sqrt{2^{1/n}}-1$

Where, $f_H(n)$=Higher 3 db frequency of identical cascaded stages

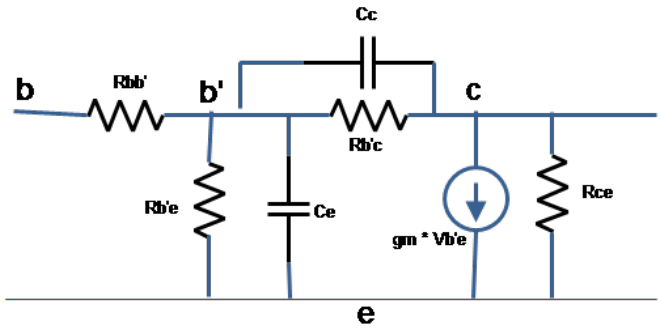
f_H=Higher 3 db frequency of single stage

n=Number of stages

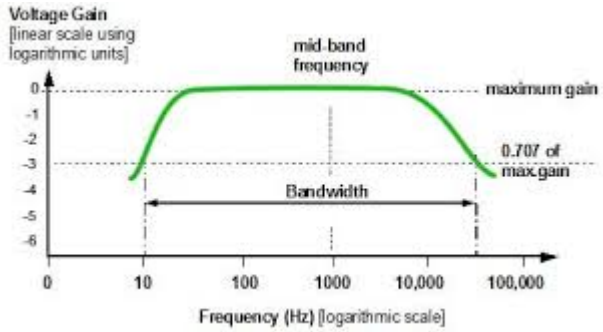
13) What is the gate capacitance in MOSFET? [CO4-L2]

It is a parallel plate capacitance formed by a gate electrode with the channel, with the oxide layer acts a capacitor dielectric. it is denoted as c_{ox}

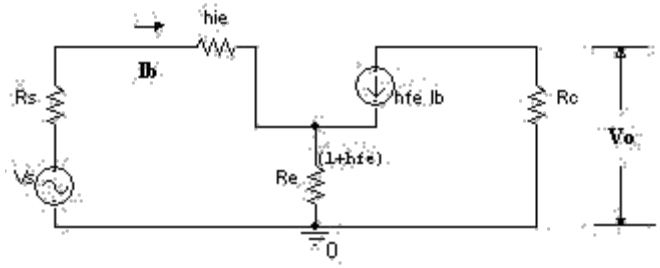
14. Draw a hybrid –pi model for a BJT? [CO4-L2]



15) Draw the general frequency response of an amplifier [CO4-L2]



16. Draw the low frequency simplified h-parameter model of an amplifier with a un bypassed emitter resistor. [CO4-L2]



17. Why an NPN transistor has a better high frequency response than the PNP transistor? [CO4-L3]

An NPN transistor has a better frequency response than the PNP transistor because the mobility of electron is more and capacitive effect is less.

18. Define f_T and f. [CO4-L2]

Unity gain frequency (f_T) or frequency parameter. It is defined as the frequency at which the common emitter shirt circuit current gain has dropped to unity and is denoted by the symbol (f_T)

19. Beta cut-off frequency (f_T). [CO4-L1]

It is defined as the high frequency at which -of a CE transistor drops to 0.707 or 3dB from its lower frequencies

20. What is the need for having a high value of f_T? [CO4-L2]

Bandwidth of the amplifier is directly proportional to f_T. Hence tp have larger bandwidth, the value of fT should be high.

21. Why N-channel FET's have a better response than P-channel FET's?

N-channel FET has a better high frequency response than P-channel FET due to the following reason.

- Mobility of electrons is large in N-channel FET whereas the mobility of holes is

poor in P-channel FET

- The input noise is less in N-channel FET that that of the P-channel FET
- The transconductance is larger in N-channel FET that that of P-channel FET

22. What is dominant network? [CO4-L2]

In high frequency analysis of an amplifier, the network having lower critical frequency is called dominant network.

23. **What is the function of Miller input capacitance of an amplifier? [CO4-L2]**

The Miller input capacitance of an amplifier is a function of Bypass capacitor.

24. What **is the use of source bypass capacitor in CS amplifier? [CO4-L1]**

Source bypass capacitor in CS amplifier is used for improving the voltage gain.

25. **Give two advantages of common source FET amplifier? [CO4-L1]**

- Good voltage gain
- High input impedance.

26. **What are the advantages of representation of gain in decibels? [CO4-L2]**

- In multistage amplifier, it permits to add individual gains of the stages to calculate overall gain.
- It allows us to denote, both very small as well as very large quantities of linear scale by considerably small figures.

27. **Write the relation between the sag and lower cut-off frequency. [CO4-L3]**

The tilt of sag in time t1 is given by

$$f_L = Pf$$

F = input signal frequency

28. Give the voltage gain for CE configuration including source resistance. **[CO4-L3]**

$$A_{vs} = \frac{\quad}{\quad} = \frac{\quad}{\quad} \quad \text{——}$$

.

29. Why thermal runaway is not there in MOSFETs? (NOV/DEC-2005) [CO4-L3]

MOSFET is temperature dependent. In MOSFET, as temperature increases drain resistance also increases', reducing the drain current. So thermal runaway does not occur in MOSFET.

30. Define transconductance? [CO4-L3]

The change in the drain current due to change in gate to source voltage can be determined using the transconductance factor gm. ΔId=gm ΔVGS

31. List the various gate capacitances in MOSFET? [CO4-L1]

There are three gate capacitances in MOSFET , that are C_{gs} , c_{gd} , c_{gb}

32. Define coupling capacitor? [CO4-L2]

The coupling capacitor c_s, couples the output of the amplifier to the load or to the next stage of the amplifier. It blocks dc and passes only ac part of the amplified signal.

33. Define current gain [CO4-L3]

The ratio of output current to input current is called current gain, A_I, of the amplifier. $A_I = I_2 / I_1$.

34. Define voltage gain [CO4-L2]

The ratio of output voltage to input voltage is called voltage gain A_V , of the amplifier. $A_V = V_2 / V_1$

35. Define benefits of h-parameter. [CO4-L3]

- Real numbers at audio frequencies
- Easy to measure
- Can be obtained from the transistor static characteristic curves
- Convenient to use in circuit analysis and design.
- Most of the transistor manufacturers specify the h-parameter.

36. What are the techniques used to improve input impedance. [CO4-L3]

- Using direct coupling (Darlington connection)
- Using Bootstrap techniques

37. Why the Darlington connection is not possible for more number of stages? [CO4-L3]

In Darlington connection of two transistors, emitter of the first transistor is directly connected to the base of the second transistor. Because of direct coupling dc output current of the first stage is (1+hfe)Ib1. If Darlington connection for n stage is (1+hfe)n times I_{b1}. Due to very large amplification factor even tow stage Darlington connection has large output current and output stage may have to be a power stage. As power amplifiers are not used in the amplifier circuits it is not possible to use more than two transistors in the Darlington connection.

38.Briefly explain why dominant pole high frequency compensation method used in amplifiers. *(May,07)* **[CO4-L2]**

- As the noise frequency components are outside the smaller bandwidth, the noise immunity of the system improves.
- Adjusting value of f_d adequate phase margin and stability of the system is assured.

Part- B

1) With neat sketch explain hybrid-pi CE transistor model. Derive the expression for various components in terms of h-parameters? [CO4-H2]

Common emitter circuit is most important practical configuration and this is useful for the analysis of transistor using hybrid - ∏ model. The following figure shows the hybrid - ∏ model for a transistor in CE configuration. For this model, all parameters are assumed to be independent of frequency. But they may vary with the quiescent operating point.

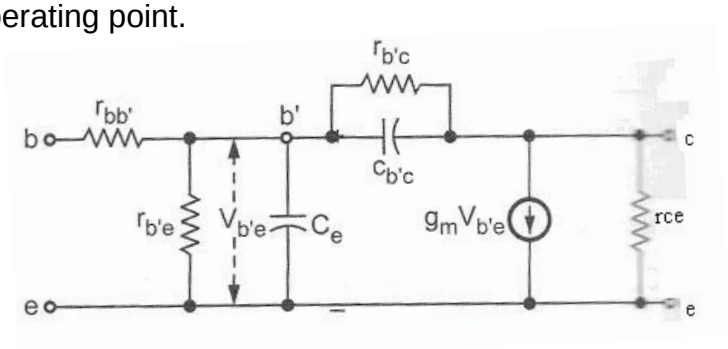


Fig. Hybrid - ∏ model for a transistor in CE configuration

Elements in hybrid – π model:

$C_{b'e}$ and $C_{b'c}$: Forward biased PN junction exhibits a capacitive effect called diffusion capacitance. This capacitive effect of normally forward biased base-emitter junction of the transistor is represented by $C_{b'e}$ or C_e. The diffusion capacitance is connected between b' and e represents the excess minority carrier storage in the base.

The reverse bias PN junction exhibits a capacitive effect called transition capacitance. This capacitive effect of normally reverse biased collector base junction of the transistor is represented by $C_{b'c}$ or C_c. **$r_{bb'}$:** The internal node b' is physically not accessible bulk node b represents external base terminal.

$r_{b'e}$: It is the portion of the base emitter which may be thought of as being in series with the collector junction. This establishes a virtual base b' for junction capacitances to be connected instead of b.

$r_{b'c}$: Due to early effect, varying voltages across collector to emitter junction results in base-width modulation. A change in the effective base -width causes the emitter current to change. This feedback effect between output and input is taken into account by connecting $g_{b'c}$ or $r_{b'c}$ between b' and c.

g_m: Due to small changes in voltage $V_{b'e}$ across emitter junction, there is excess minority carrier concentration injected into the base which is proportional to $V_{b'e}$. So resulting small signal collector current with collector shorted to the emitter is also proportional to

Vb'e.

g_m is also called as transconductance and it is given as,

$$g_m = \frac{\Delta I_C}{\Delta V_{b'e}} \text{ at a constant } V_{CE}$$

r_{ce}: It is the output resistance. It is also the result of early effect.

4.4.1.2 Hybrid – π parameter values:

The following table shows the typical values for hybrid - π parameters at room temperature and for I_c = 1.3mA.

Parameter	Meaning	Value
g_m	Mutual conductance	50mA/V
rbb'	Base spreading resistance	100Ω
rb'e or gb'e	Resistance between b' and e	1kΩ
	Conductance between b' and e	1m mho
rb'c or gb'c	Resistance of reverse biased PN junction between base and collector	4MΩ
	Conductance of reverse biased PN junction between base and collector	$0.25*10^{-6}$ mho
r_{ce} or g_{ce}	Output resistance between c and e	80kΩ
	Conductance between c and e	$12.5*10^{-6}$ mho
C_e	Junction capacitance between b and e	100pF
C_c	Junction capacitance between base and Collector	3pF

Hybrid – π conductances

Transistor Transconductance g_m:

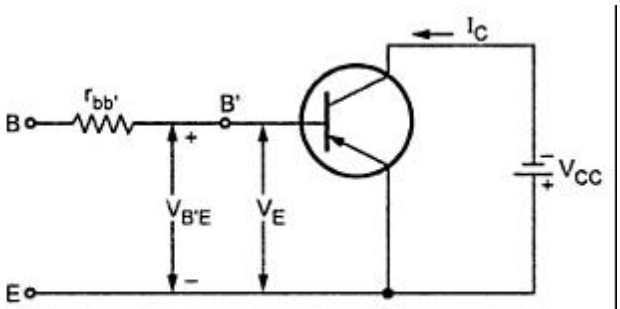


Fig. Pertaining to the derivation of g_m

Let us consider a p-n-p transistor in CE configuration with V_{cc} bias in the collector circuit as shown in the above figure.

Transconductance g_m is given as,

$$g_m = \left.\frac{\partial I_C}{\partial V_{B'E}}\right|_{V_{CE}}$$

The collector current in active region is given as,

$$I_C = I_{CO} - \alpha I_E$$

$$\partial I_C = \alpha \, \partial I_E \quad \because I_{CO} = \text{constant.}$$

Substituting value of ∂I_C

$$g_m = \alpha \frac{\partial I_E}{\partial V_{B'E}} = \alpha \frac{\partial I_E}{\partial V_E} \quad \because V_E = V_{B'E}$$

The emitter diode resistance, r_e is given as,

$$r_e = \frac{\partial V_E}{\partial I_E}$$

$$\frac{1}{r_e} = \frac{\partial V_E}{\partial I_E}$$

Substituting r_e in place of $\partial I_E / \partial V_E$ we get,

$$g_m = \frac{\alpha}{r_e}$$

The emitter diode is a forward biased diode and its dynamic resistance is given as,

$$r_e = \frac{V_T}{I_E}$$

The emitter diode is a forward biased diode and its dynamic resistance is given as,

$$r_e = \frac{V_T}{I_E}$$

where V_T is the "volt equivalent of temperature", defined by

$$V_T = \frac{KT}{q}$$

where K is the Boltzmann constant in joules per degree kelvin (1.38×10^{-23} J/°K) is the electronic charge (1.6×10^{-19} C).

Substituting value of r_e in equation (3) we get,

$$g_m = \frac{\alpha I_E}{V_T} = \frac{I_{CO} - I_C}{V_T} \quad \because I_C = I_{CO} - \alpha I_E$$

For p-n-p transistor I_C is negative. For an n-p-n transistor I_C is positive, but the foregoing analysis (with $V_E = +V_{BE}$) leads to $g_m = (I_C - I_{CO}) / V_T$.

Hence, for either type of transistor, g_m is positive.

$$g_m = \frac{I_C - I_{CO}}{V_T} \quad \because I_C >> I_{CO}$$

For I_c = 1.3mA, g_m = 0.05mho or 50 mA/V. For I_c = 7.8mA, g_m = 0.3mho or 300mA/V. These values are much larger than the transconductances obtained with FETs.

Input Conductance $g_{b'e}$:

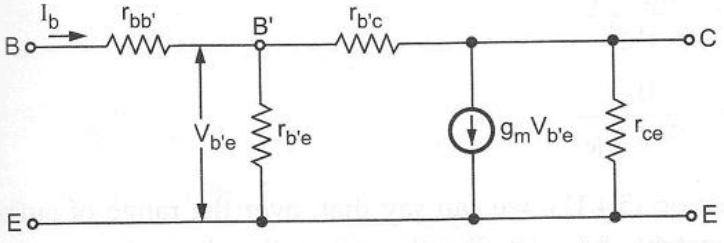


Fig. Hybrid - π model for CE configuration at low frequency

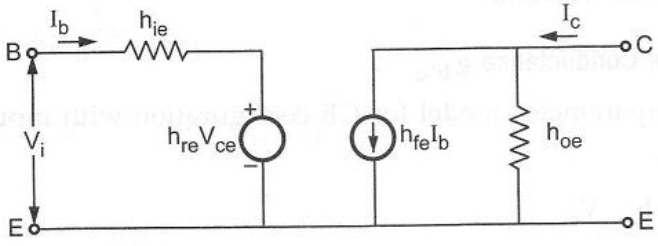


Fig. h-parameter model for CE configuration at low frequency

First consider h-parameter model for CE configuration. Applying KCL to output circuit,

$$I_C = h_{fe} I_b + h_{oe} V_{ce}$$

Making $V_{ce} = 0$, the short circuit current gain h_{fe} is defined as,

Substituting the value of I_C / I_b,

$$h_{fe} = g_m \; r_{b'e}$$

or

$$r_{b'e} = \frac{h_{fe}}{g_m} \quad \text{or} \quad g_{b'e} = \frac{g_m}{h_{fe}}$$

$$g_m = I_C / V_T \qquad I_b \; r_{b'e}.$$

$$\therefore \quad r_{b'e} = \frac{h_{fe} V_T}{|I_C|}$$

$$\text{or} \quad g_{b'e} = \frac{|I_C|}{V_T \; h_{fe}}$$

Feedback Conductance $g_{b'c}$:

Let us consider h-parameter model for CE configuration with input open circuit ($I_b = 0$), V_i is given as,

$$V_i = h_{re} V_{ce}$$

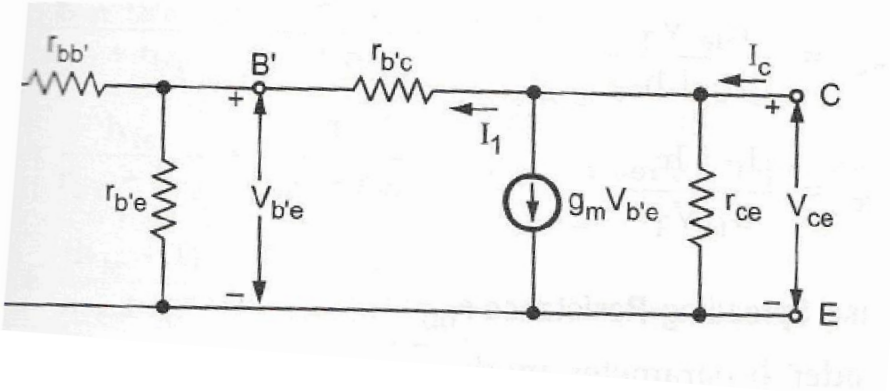


Fig. Hybrid –π model for CE configuration

With $I_b = 0$, V_{ce} is given as,

$V_{ce} = I_1 (r_{b'c} + r_{b'e})$

$$I_1 = \frac{V_{ce}}{r_{b'c} + r_{b'e}}$$

Voltage between b' and e, $V_{b'e}$ can be given as,

$$Vb'e = I_1 r_{b'e}$$

$$= r_{b'e} \frac{V_{ce}}{r_{b'c} + r_{b'e}}$$

With $I_b = 0$,

$Vi = Vb'e$

$$= \frac{r_{b'e} V_{ce}}{r_{b'c} + r_{b'e}}$$

Substituting the value of V_i,

$$\frac{r_{b'e} V_{ce}}{r_{b'c} + r_{b'e}}$$

$$= \frac{r_{b'e}}{r_{b'c} + r_{b'e}}$$

$$hreVce = h_{re} r_{b'c} + h_{re} r_{b'e}$$

$$= \left(\frac{1 - h_{re}}{h_{re}}\right) r_{b'e}$$

rb'c = $= \frac{r_{b'e}}{h_{re}} \quad \because 1 - h_{re} \approx 1$

$$g_{b'c} = \frac{h_{re}}{r_{b'e}} = h_{re}\, g_{b'e}$$

Base Spreading Resistance $r_{bb'}$:

$$r_{b'c} = \frac{h_{fe}\, V_T}{|I_C|\, h_{re}}$$

$$|I_C|\, h_{re}$$

$$h_{ie} = r_{bb'} + r_{b'e} \quad T$$

$$r_{bb'} = h_{ie} - r_{b'e}$$

Substituting the value of $r_{b'e}$,

$$r_{bb'} = h_{ie} - \frac{h_{fe}\, V_T}{I_C}$$

Output Resistance g_{ce}:

Using h-parameters output conductance is given as,

$$h_{oe} = \frac{I_C}{V_{ce}}$$

Applying KCL to the output circuit,

$$I_C = \frac{V_{ce}}{r_{ce}} + g_m\, V_{b'e} + I_1$$

$$h_{oe} - g_{b'c} h_{fe}$$

2) Discuss the frequency response of multistage amplifiers. calculate the overall upper and lower cut off frequency? [CO4-H3]

Frequency Response of Multistage Amplifiers:

The bandwidth of multistage amplifier is always less than that of the bandwidth of single stage amplifier.

Overall Lower Cut-off Frequency of Multistage Amplifier:

Let us consider the lower 3dB frequency of n identical cascaded stages as f_L (n). It is the frequency for which the overall gain falls to 1/√2 (3dB) of its midband value.

$$\left[\frac{1}{\sqrt{1+\left(\frac{f_L}{f_L(n)}\right)^2}}\right]^n = \frac{1}{\sqrt{2}}$$

$$\sqrt{2} = \left[\sqrt{1+\left(\frac{f_L}{f_L(n)}\right)^2}\right]^n$$

Squaring on both the sides &

Taking n^{th} root on both sides we get,

$$2^{\frac{1}{n}} = 1+\left(\frac{f_L}{f_L(n)}\right)^2$$

$$2^{\frac{1}{n}} - 1 = \left(\frac{f_L}{f_L(n)}\right)^2$$

Taking square root on both the sides,

$$\sqrt{2^{1/n} - 1} = \frac{f_L}{f_L(n)}$$

$$f_L(n) = \frac{f_L}{\sqrt{2^{1/n} - 1}}$$

where $f_L(n)$ = Lower 3 dB frequency of identical cascaded stages

f_L = Lower 3 dB frequency of single stage

n = Number of stages

Overall Higher Cut-off Frequency of Multistage Amplifier:

Let us consider the upper 3dB frequency of n identical cascaded stages as $f_H(n)$. It is the frequency for which the overall gain falls to $1/\sqrt{2}$ (3dB) of its midband value.

$$\left[\frac{1}{\sqrt{1+\left(\frac{f_H(n)}{f_H}\right)^2}}\right]^n = \frac{1}{\sqrt{2}}$$

$$\sqrt{2} = \left[\sqrt{1+\left(\frac{f_H(n)}{f_H}\right)^2}\right]^n$$

Squaring both the sides,

$$2 = \left[1+\left(\frac{f_H(n)}{f_H}\right)^2\right]^n$$

Taking n^{th} root on both the sides,

$2^{1/n} = 1 + [f_H(n)/f_H$

$]^2$ $2^{1/n}$ -1 = [$f_H(n)/f_H$

$]^2$

Taking square root on both the sides,

$\sqrt{2^{1/n}}$ -1 =

$f_H(n)/f_H$ $f_H(n)$ =

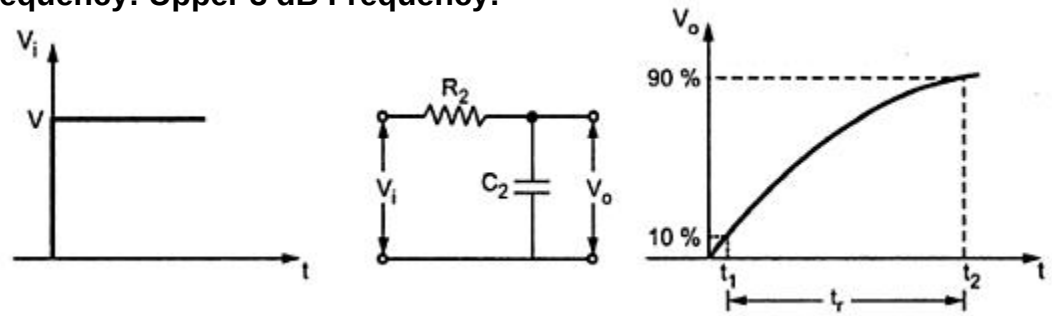
$f_H \sqrt{2^{1/n}}$ -1

In multistage amplifier $f_L(n)$ is always greater than f_L and $f_H(n)$ is always less than $f_{H.}$ So the bandwidth of multistage amplifier is always less than single stage amplifier.

If stages are not identical f_H can be given as,

$$\frac{1}{f_H} = 1.1\sqrt{\frac{1}{f_1^2}+\frac{1}{f_2^2}+\cdots+\frac{1}{f_n^2}}$$

Rise time and its Relation to Upper Cut-off Frequency: Upper 3 dB Frequency:



When a step input is applied, amplifier high frequency RC network prevent the output from responding immediately to the step input. The output voltage starts from zero and rises towards the steady state value V, with a time constant R_2C_2 as shown in the above figure.

The output voltage is given by,

$$V_o = V(1 - e^{-t_1/R_2 C_2})$$

The time required for V_o to reach one-tenth of its final value is calculated as,

The time required for V_o to reach one-tenth of its final value is calculated as,

$$0.1\ V = V\ (1 - e^{-t_1/R_2 C_2})$$

$$\therefore \quad 0.1 = 1 - e^{-t_1/R_2 C_2}$$

$$\therefore \quad 0.9 = e^{-t_1/R_2 C_2}$$

$$\therefore \quad \frac{t_1}{R_2 C_2} = 0.1$$

$$\therefore \quad t_1 = 0.1\ R_2 C_2$$

Similarly, the time required for V_o to reach nine-tenths of its final value is calculated as,

$$0.9\ V = V\ (1 - e^{-t_2/R_2 C_2})$$

$$\therefore \quad 0.9 = 1 - e^{-t_2/R_2 C_2}$$

$$\therefore \quad 0.1 = e^{-t_2/R_2 C_2}$$

$$\therefore \quad \frac{t_2}{R_2 C_2} = 2.3$$

The difference between these two values is called as rise time t_r of the circuit. The rise time is given as,

$$t_r = t_2 - t_1 = 2.3\ R_2 C_2 - 0.1\ R_2 C_2$$
$$= 2.2\ R_2 C_2$$

The Upper 3dB frequency is given as,

$$f_H = \frac{1}{2\pi R_2 C_2}$$

Upper 3dB frequency in terms of rise time is given as

$$f_H = \frac{2.2}{2\pi t_r} = \frac{0.35}{t_r}$$

From above equation, it shows that upper 3dB frequency is inversely proportional to the rise time t_r.

Relation between Bandwidth and Rise time:

The frequency range from f_L to f_H is called bandwidth of the amplifier. Usually $f_L << f_H$. So we can approximate the equation for bandwidth as follows,

$$BW = f_H - f_L$$
$$\approx f_H$$

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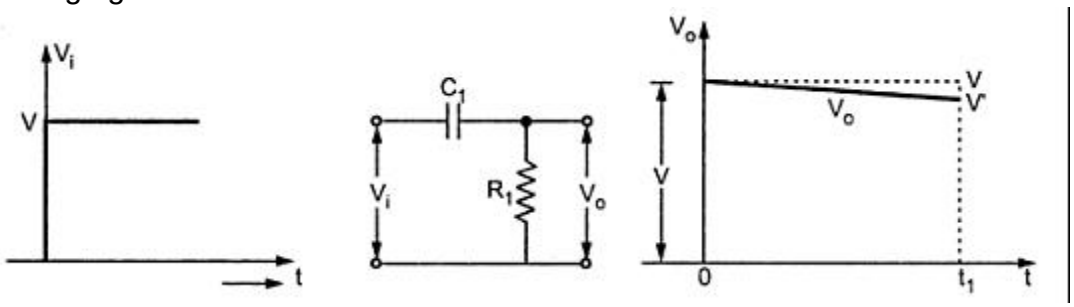
Sag and its Relation to Lower Cut-off Frequency:

The amplifier low frequency RC network consists of coupling and bypass capacitors make amplifier output to decrease with large time constant. As a result, the output voltage has sag or tilt associated with it as shown in the following figure.



The tilt or sag in time t_1 is given by,

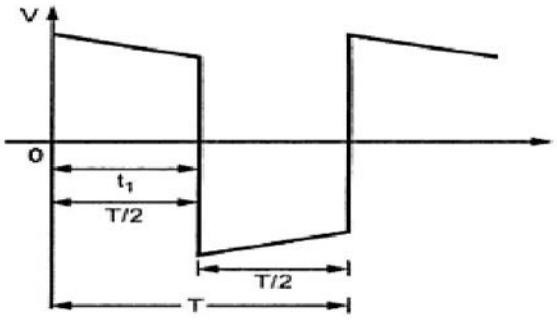
$$\% \text{ tilt} = P = \frac{V - V'}{V} \times 100$$
$$= \frac{t_1}{R_1 C_1} \times 100 \%$$

The lower 3 dB frequency can be determined from the output response by carefully measuring the tilt.

The lower 3 dB frequency is given as

$$f_L = \frac{1}{2\pi R_1 C_1}$$

So, the lower 3 dB frequency can be represented in terms of tilt is measured from the following figure.



$$P = \frac{T}{2R_1C_1} \times 100$$

$$= \frac{1}{2fR_1C_1} \times 100 \qquad \because T = \frac{1}{F}$$

$$= \frac{\pi}{2\pi f R_1C_1} \times 100$$

3) Discuss the low frequency and the high frequency response of amplifiers. Derive its cut off frequencies? [CO4-H1]

General shape of frequency response of amplifiers

An audio frequency amplifier which operates over audio frequency range extending from 20 Hz to 20 kHz .Audio frequency amplifiers are used in radio receivers, large public meeting and various announcements to be made for the passengers on railway platforms. Over the range of frequencies at which it is to be used an amplifier should ideally provide the same amplification for all frequencies. The degree to which this is done is usually indicated by the curve known as frequency response curve of the amplifier.

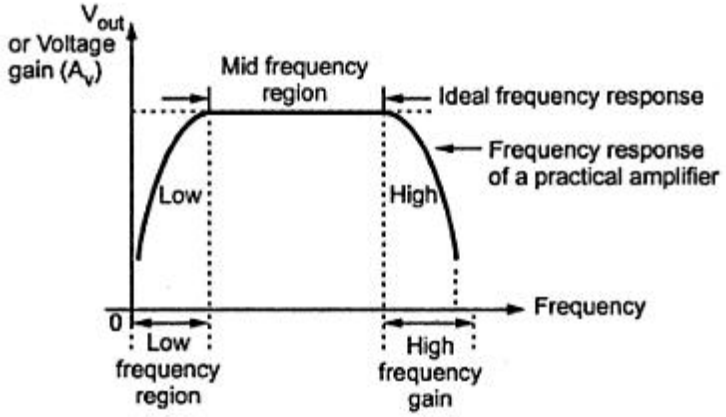


Fig. A typical frequency response of an amplifier

To plot this curve, input voltage to the amplifier is kept constant and frequency of input signal is continuously varied. The output voltage at each frequency of input signal is noted and the gain of the amplifier is calculated. For an audio frequency amplifier, the frequency range is quite large from 20 Hz to 20 kHz. In this frequency response, the gain of the amplifier remains constant in mid-frequency while the gain varies with frequency in low and high frequency regions of the curve. Only at low and high frequency ends, gain deviates from ideal characteristics. The decrease in voltage gain with frequency is called roll-off.

Definition of cut-off frequencies and bandwidth:

The range of frequencies can be specified over which the gain does not deviate more than 70.7% of the maximum gain at some reference mid-frequency.

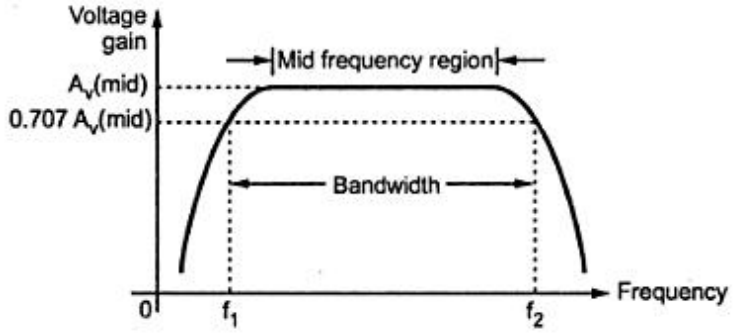


Fig. Frequency response, half power frequencies and bandwidth of an RC coupled amplifier

From above figure, the frequencies f_1 & f_2 are called lower cut-off and upper cut-off frequencies.

Bandwidth of the amplifier is defined as the difference between f_2 & f_1. Bandwidth of the amplifier = $f_2 - f_1$

The frequency f_2 lies in high frequency region while frequency f_1 lies in low frequency region. These two frequencies are also called as half-power frequencies since gain or output voltage drops to 70.7% of maximum value and this represents a power level of one half the powers at the reference frequency in mid-frequency region.

4. Discuss about Low frequency analysis of amplifier to obtain lower cut-off frequency: [CO4-H3]

Decibel Unit:

The decibel is a logarithmic measurement of the ratio of one power to another or one voltage to another. Voltage gain of the amplifier is represented in decibels (dBs). It is given by,

Voltage gain in dB = 20 log

A_v Power gain in decibels is given by,

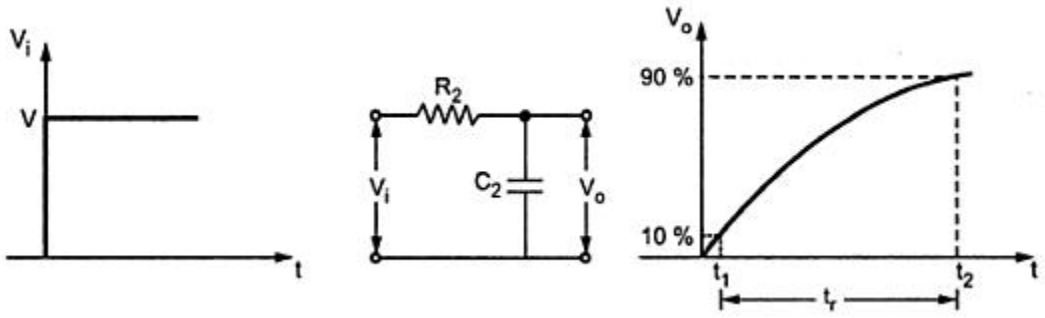
Power gain in dB = 10 log A_p

Where A_v is greater than one, gain is positive and when A_v is less than one, gain is negative. The positive and negative gain indicates that the amplification and attenuation respectively. Usually the maximum gain is called mid frequency range gain is assigned a 0 db value. Any value of gain below mid frequency range can be referred as 0 db and expressed as a negative db value.

5. Discuss the terms raise time and sag? [CO4-H21

Rise time and its Relation to Upper Cut-off Frequency:

Upper 3 dB Frequency:



When a step input is applied, amplifier high frequency RC network prevent the output from responding immediately to the step input. The output voltage starts from zero and rises towards the steady state value V, with a time constant R_2C_2 as shown in the above figure.

The output voltage is given by,

$$V_o = V(1 - e^{-t_1/R_2 C_2})$$

The time required for V_o to reach one-tenth of its final value is calculated as,

The time required for V_o to reach one-tenth of its final value is calculated as,

$$0.1\ V = V\ (1 - e^{-t_1/R_2 C_2})$$

$$\therefore \quad 0.1 = 1 - e^{-t_1/R_2 C_2}$$

$$\therefore \quad 0.9 = e^{-t_1/R_2 C_2}$$

$$\therefore \quad \frac{t_1}{R_2 C_2} = 0.1$$

$$\therefore \quad t_1 = 0.1\ R_2 C_2$$

Similarly, the time required for V_o to reach nine-tenths of its final value is calculated as,

$$0.9\ V = V\ (1 - e^{-t_2/R_2 C_2})$$

$$\therefore \quad 0.9 = 1 - e^{-t_2/R_2 C_2}$$

$$\therefore \quad 0.1 = e^{-t_2/R_2 C_2}$$

$$\therefore \quad \frac{t_2}{R_2 C_2} = 2.3$$

The difference between these two values is called as rise time t_r of the circuit. The rise time is given as,

$$t_r = t_2 - t_1 = 2.3\ R_2 C_2 - 0.1\ R_2 C_2$$
$$= 2.2\ R_2 C_2$$

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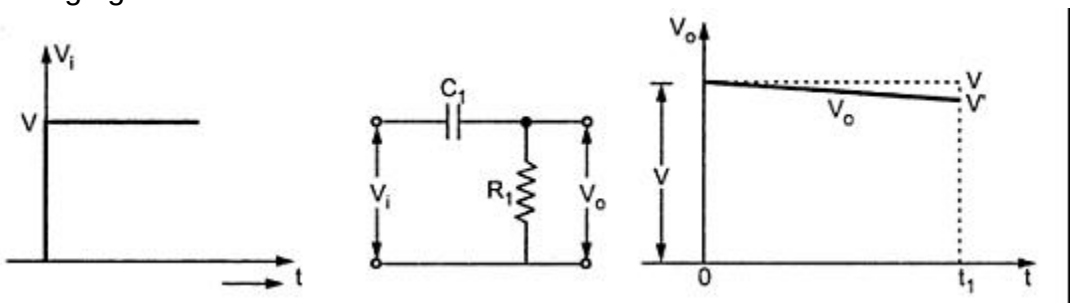

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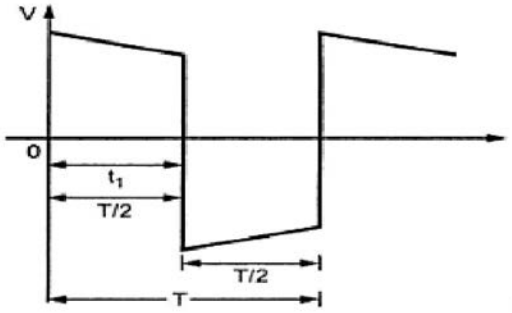

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$$= \frac{1}{2fR_1C_1} \times 100 \qquad \because T = \frac{1}{F}$$

$$= \frac{\pi}{2\pi f R_1 C_1} \times 100$$

5. Derive the expression for the CE short current gain of transistor at high frequency? [CO4-H3]

CE short circuit current gain using hybrid- π model:

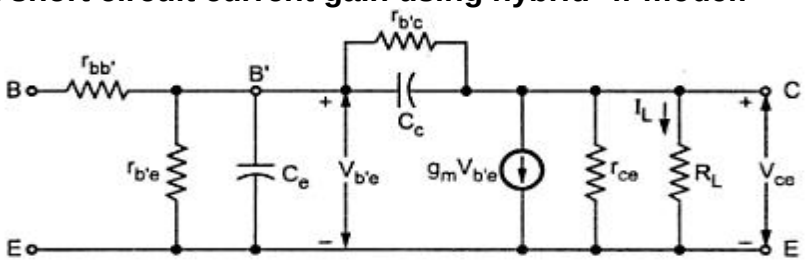


Fig. Hybrid- π model for a single transistor with a resistive load R_L

Miller capacitance is $C_M = C_{b'c}\,(1 + g_m\,R_L)$

Here, $R_L = 0$

$\therefore \quad C_M = C_{b'c}\,(C_c)$

Parallel combination of $r_{b'e}$, and $(C_e + C_c)$ is given as

$$Z = \frac{r_{b'c} \times \dfrac{1}{j\omega(C_e + C_c)}}{r_{b'e} + \dfrac{1}{j\omega(C_e + C_c)}}$$

$$= \frac{r_{b'e}}{1 + j\omega\, r_{b'e}\,(C_e + C_c)}$$

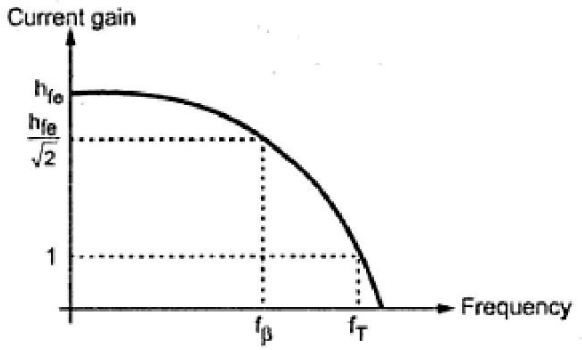
The current gain for the circuit is,

$$A_i = \frac{I_L}{I_b} = \frac{-g_m\,V_{b'e}}{I_b} \qquad \because I_L = -\,g_m V_{b'e}$$

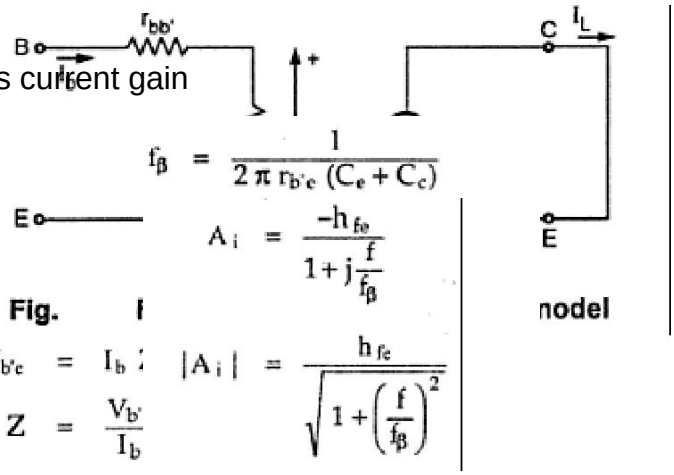
$$A_i = -g_m\,Z$$

$$= \frac{-g_m\,r_{b'e}}{1 + j\omega\, r_{b'e}\,(C_e + C_c)}$$

$$A_i = \frac{-h_{fe}}{1 + j\omega\, r_{b'e}\,(C_e + C_c)}$$



Frequency vs current gain



$$f_\beta = \frac{1}{2\pi r_{b'e}(C_e + C_c)}$$

$$A_i = \frac{-h_{fe}}{1 + j\frac{f}{f_\beta}}$$

Fig. nodel

$$V_{b'e} = I_b \quad |A_i| = \frac{h_{fe}}{\sqrt{1 + \left(\frac{f}{f_\beta}\right)^2}}$$

$$Z = \frac{V_{b'}}{I_b}$$

f_β (Cutoff frequency):

It is the frequency at which the transistor short circuit CE current gain drops by 3dB or 1/√√2 times from its value at low frequency. It is given as,

$$f_\beta = \frac{1}{2\pi r_{b'e}(C_e + C_c)}$$

or

$$= \frac{g_{b'e}}{2\pi(C_e + C_c)}$$

or

$$= \frac{1}{h_{fe}} \frac{g_m}{2\pi(C_e + C_c)} \quad \because g_{b'e} = \frac{1}{r_{b'e}} = \frac{g_m}{h_{fe}}$$

f_α (Cut-off frequency):

It is the frequency at which the transistor short circuit CB current gain drops by 3dB or 1/√√2 times from its value at low frequency.

The current gain for CB configuration is given as

$$A_i = \frac{-h_{fb}}{1 + j\frac{f}{f_\alpha}}$$

where $$f_\alpha = \frac{1}{2\pi r_{b'e}(1 + h_{fb})C_e}$$

$$= \frac{1 + h_{fe}}{2\pi r_{b'e} C_e} \approx \frac{h_{fe}}{2\pi r_{b'e} C_e}$$

$$|A_i| = \frac{h_{fb}}{\sqrt{1 + \left(\frac{f}{f_\alpha}\right)^2}}$$

At $f = f_\alpha$

$$|A_i| = \frac{h_{fb}}{\sqrt{2}}$$

Parameter f_T:

It is the frequency at which short circuit CE current gain becomes unity.

At $f = f_T$,

$$1 = \frac{h_{fe}}{\sqrt{1+\left(\frac{f_T}{f_\beta}\right)^2}}$$

The ratio of f_T / f_β is quite large compared to 1.

$$f_T = g_m / 2\pi C_e$$

Current gain with resistive load:

$$C_{eq} = C_e + C_c (1 + g_m R_L)$$

For further simplification,

At output circuit value of C_c can be calculated as,

$$\frac{-h_{fe}}{1+j\left(\frac{f}{f_H}\right)}$$

Simplified hybrid – π model for CE with R_L

$$Z = \frac{V_{b'e}}{I_b}$$

$$|A_i| = \frac{h_{fe}}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}}$$

At $f = f_H$

$$A_i = \frac{h_{fe}}{\sqrt{2}}$$

f_H is the frequency at which the transistor gain drops by 3dB or 1/√2 times from its value at low frequency. It is given as,

$$f_H = \frac{1}{2\pi r_{b'e} C_{eq}}$$

$$= \frac{1}{2\pi r_{b'e} [C_e + C_c (1 + g_m R_L)]}$$

At $R_L = 0$

$$f_H = \frac{1}{2\pi r_{b'e} [C_e + C_c]} = f_\beta$$

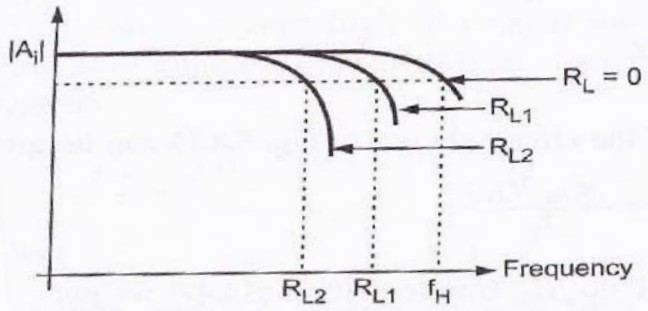


Fig. Variation f_H with R_L

Current gain including source resistance:

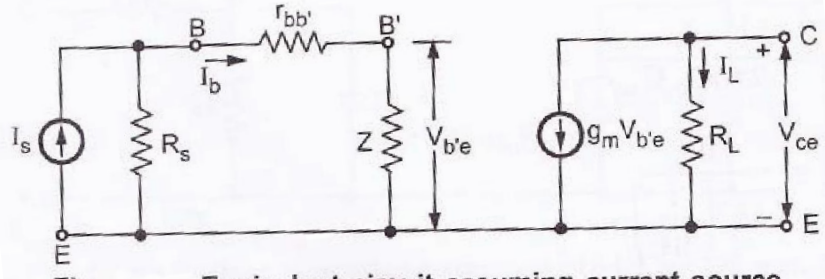


Fig. Equivalent circuit assuming current source

$$\frac{I_L}{I_s} = \frac{-g_m r_{b'e} R_s}{R_s + r_{bb'} + r_{b'e}}$$

A_{is} at low frequency =

$$\frac{- h_{fe} R_S}{R_s + h}$$

6) Discuss the frequency response of MOSFET CS amplifiers? [CO4-H2]

Frequency Response of Common Source Amplifier:

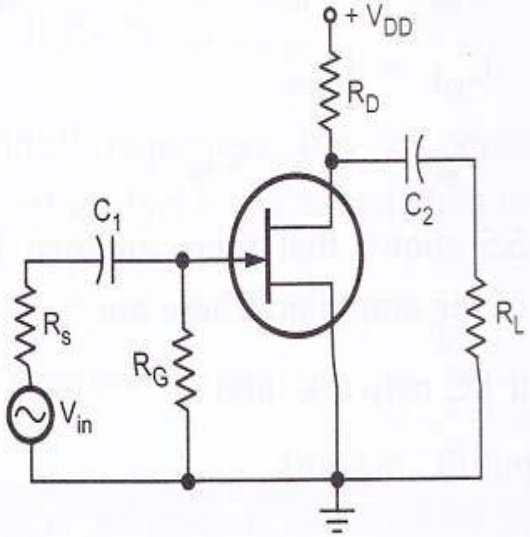


Fig. Typical RC coupled common source amplifier

Let us consider a typical common source amplifier as shown in the above figure.

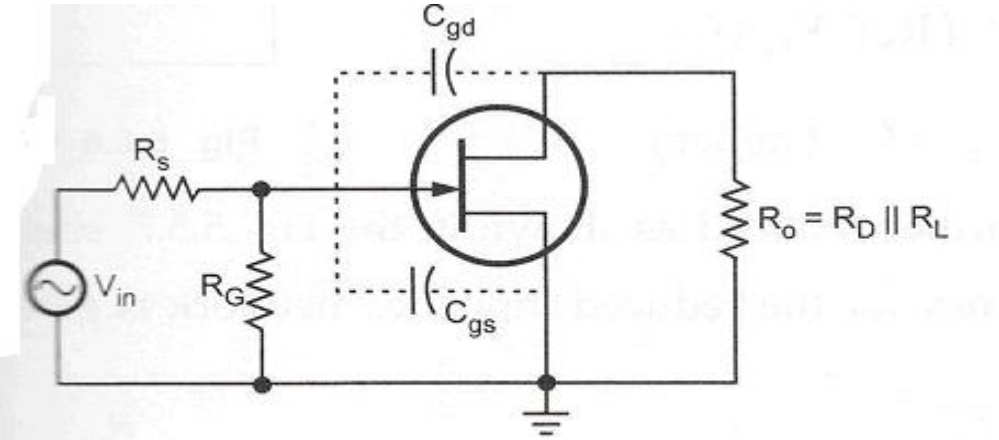


Fig. High frequency equivalent circuit

From above figure, it shows the high frequency equivalent circuit for the given amplifier circuit. It shows that at high frequencies coupling and bypass capacitors act as short circuits and do not affect the amplifier high frequency response. The equivalent circuit shows internal capacitances which affect the high frequency response.

Using Miller theorem, this high frequency equivalent circuit can be further simplified as follows:

The internal capacitance C_{gd} can be splitted into $C_{in(miller)}$ and $C_{out(miller)}$ as shown in the following figure.

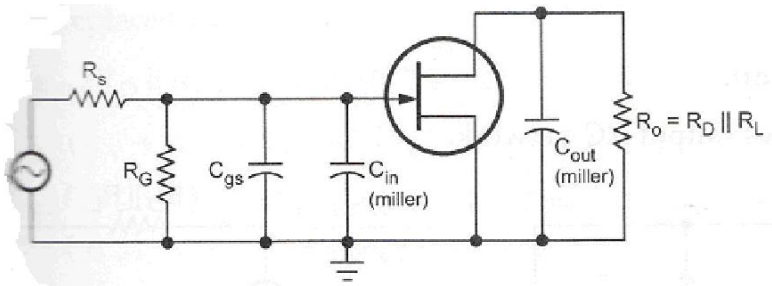


Fig. Simplified high frequency equivalent circuit

$$C_{in\,(miller)} = C_{gd}\,(A_v + 1)$$

$$C_{out\,(miller)} = C_{gd}\,\frac{(A_v + 1)}{(A_v)}$$

Where

$$C_{gd} = C_{rss}$$

$$C_{gs} = C_{iss} - C_{rss}$$

From simplified high frequency equivalent circuit, it has two RC networks which affect the high frequency response of the amplifier. These are,

1. Input RC network
2. Output RC network

Input RC network:

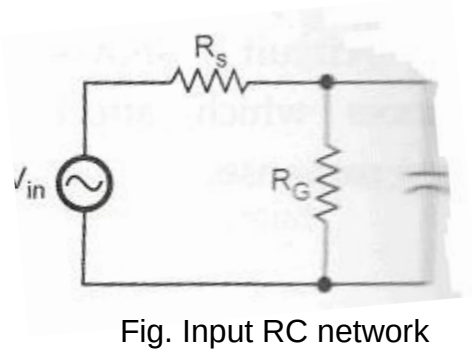


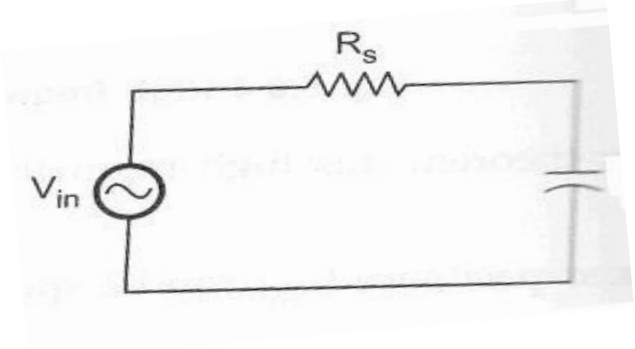
Fig. Input RC network

From above figure,

$$f_{c(input)} = \frac{1}{2\pi(R_S \,||\, R_G)\, C_T}$$

where $C_T = C_{gs} + C_{in}(\text{miller})$

This network is further reduced as follows since $R_s << R_G$



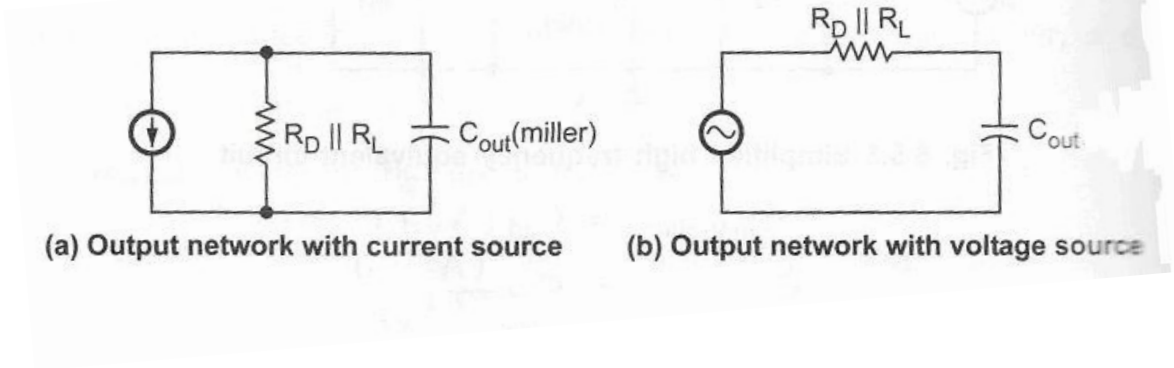
The critical frequency for the reduced input RC network is,

$$f_{c\,(input)} = \frac{1}{2\pi R_s C_T}$$

$$\text{or } f_c = \frac{1}{2\pi R_s [C_{gs} + C_{in\,(miller)}]}$$

The phase shift in high frequency RC network is $\theta = \tan^{-1}\left(\frac{R_s}{X_{C_T}}\right)$

Output RC network:



(a) Output network with current source (b) Output network with voltage source

The critical frequency for the above circuit is,

$$\frac{1}{2\pi R_o C_{out\,(miller)}} = \frac{1}{2\pi (R_D \parallel R_L) C_{out\,(miller)}}$$

f_c =

It is not necessary that these frequencies should be equal. The network which has lower critical frequency than other network is called dominant network.

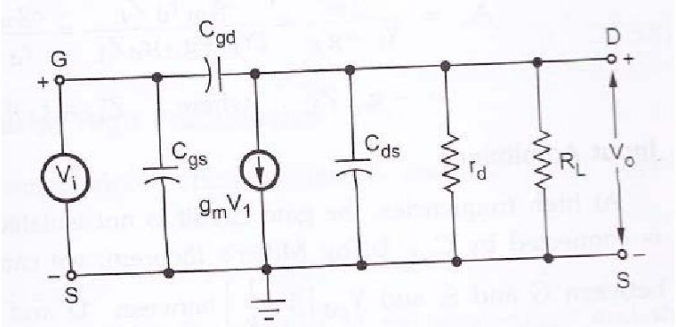
The phase shift in high frequency is

$$\theta = \tan^{-1}\left(\frac{R_o}{X_{C\,out\,(Miller)}}\right)$$

7. Discuss the gain bandwidth for high frequency FET amplifiers? [CO4-H1]

High frequency analysis of FET

Common source amplifier at high frequencies:



Small signal equivalent circuit at high frequencies

$$Y = \frac{1}{Z} = Y_L + Y_{ds} + g_d + Y_{gd}$$

where

$Y_L = \frac{1}{R_L}$: admittance corresponding to R_L

$Y_{ds} = j\omega C_{ds}$: admittance corresponding to C_{ds}

$g_d = \frac{1}{r_d}$: conductance corresponding to r_d

$Y_{gd} = j\omega C_{gd}$: admittance corresponding to C_{gd}

$$I = -g_m V_i + V_i Y_{gd} = V_i (-g_m + Y_{gd})$$

Voltage gain:

The voltage gain for common source amplifier circuit with the load R_L is given by,

$$A_v = \frac{V_o}{V_i} = \frac{IZ}{V_i} = \frac{I}{V_i Y}$$

Substituting the values of I and Y from equations (2) and (3) we have,

$$A_v = \frac{-g_m + Y_{gd}}{Y_L + Y_{ds} + g_d + Y_{gd}}$$

At low frequencies, Y_{ds} and $Y_{gd} = 0$ and hence equation (4) reduces to

$$A_v = \frac{-g_m}{Y_L + g_d} = \frac{-g_m r_d Z_L}{(Y_L + g_d) r_d Z_L} = \frac{-g_m r_d Z_L}{r_d + Z_L}$$

$$= -g_m Z_L' \qquad \text{where} \quad Z_L' = r_d \,||\, Z_L$$

Input Admittance:

$$Y_i = Y_{gs} + (1 - A_v) Y_{gd}$$

Input capacitance (Miller Effect):

$$A_v = -g_m R_d' \qquad \text{where} \quad R_d' = r_d R_d$$

Substituting the value of A_v

$$\frac{Y_i}{j\omega} \equiv C_i = C_{gs} + (1 + g_m R_d') C_{gd}$$

This increase in input capacitance C_i over the capacitance from gate to source is called Miller effect.

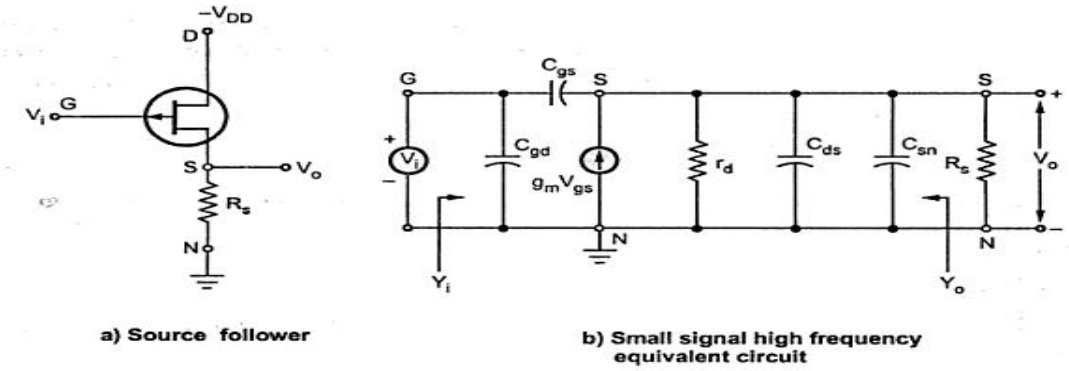
This input capacitance affects the gain at high frequencies in the operation of cascaded amplifiers. In cascaded amplifiers, the output from one stage is used as the input to a second amplifier. The input impedance of a second stage acts as a shunt across output of the first stage and R_d is shunted by the capacitance C_i.

Output Admittance

From above figure, the output impedance is obtained by looking into the drain with the input voltage set equal to zero. If $V_i = 0$ in figure, r_d , C_{ds} and C_{gd} in parallel. Hence the output admittance with R_L considered external to the amplifier is given by,

$$Y_o = g_d + Y_{ds} + Y_{gd}$$

Common Drain Amplifier at High Frequencies:



a) Source follower

b) Small signal high frequency equivalent circuit

Common Drain Amplifier Circuit & Small signal equivalent circuit at high frequencies

Voltage gain:

The output voltage V_o can be found from the product of the short circuit and the impedance between terminals S and N. Voltage gain is given by,

$$\frac{V_o}{V_i} = \frac{g_m + j\omega C_{gs}}{R_s + (g_m + g_d + j\omega C_T)}$$

where $C_T \equiv C_{gs} + C_{ds} + C_{sn}$

$$A_v = \frac{(g_m + j\omega C_{gs})R_s}{1 + (g_m + g_d + j\omega C_T)R_s}$$

At low frequencies the gain reduces to

$$A_v = \frac{g_m R_s}{1 + (g_m + g_d)R_s}$$

Input Admittance:

Input Admittance Y_i can be obtained by applying Miller's theorem to C_{gs}.

It is given by,

$$Y_i = j\omega C_{gd} + j\omega C_{gs}(1 - A_v) \approx j\omega C_{gd}$$

because $A_v \approx 1.$

Output Admittance:

Output Admittance Y_o with R_s considered external to the amplifier, it is given by,

$$Y_o = g_m + g_d + j\omega C_T$$

At low frequencies, output resistance R_o is given by,

$$R_o = \frac{1}{g_m + g_d} \approx \frac{1}{g_m} \qquad \text{since } g_m >> g_d$$

Frequency Response of Common Source Amplifier:

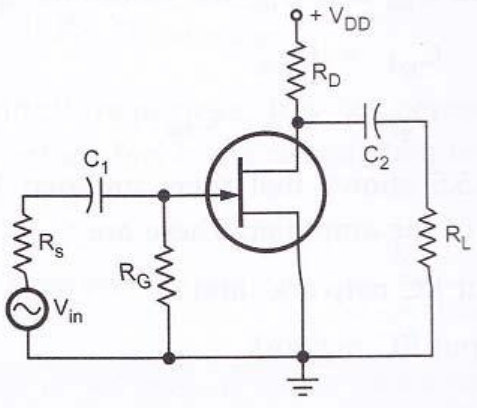


Fig. Typical RC coupled common source amplifier

Let us consider a typical common source amplifier as shown in the above figure.

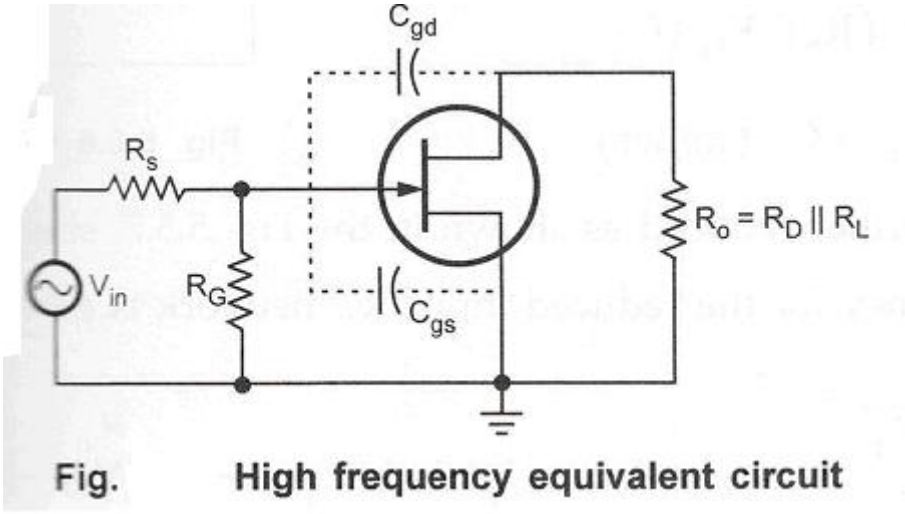


Fig. High frequency equivalent circuit

From above figure, it shows the high frequency equivalent circuit for the given amplifier circuit. It shows that at high frequencies coupling and bypass capacitors act as short circuits and do not affect the amplifier high frequency response. The equivalent circuit shows internal capacitances which affect the high frequency response.

Using Miller theorem, this high frequency equivalent circuit can be further simplified as follows:
The internal capacitance C_{gd} can be splitted into $C_{in(miller)}$ and $C_{out(miller)}$ as shown in the following figure.

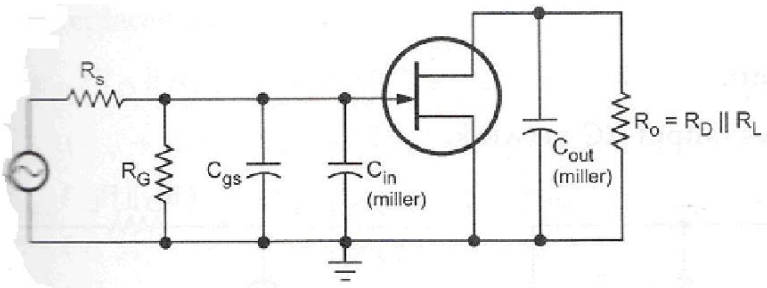


Fig. Simplified high frequency equivalent circuit

$$C_{in\,(miller)} = C_{gd}\,(A_v + 1)$$

$$C_{out\,(miller)} = C_{gd}\,\frac{(A_v + 1)}{(A_v)}$$

Where

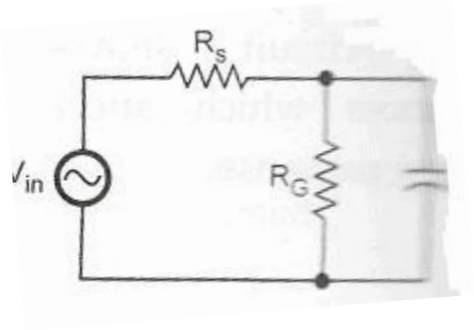
$$C_{gd} = C_{rss}$$

$$C_{gs} = C_{iss} - C_{rss}$$

From simplified high frequency equivalent circuit, it has two RC networks which affect the high frequency response of the amplifier. These are,

1. Input RC network
2. Output RC network

Input RC network:



From above figure,

$$f_{c(input)} = \frac{1}{2\pi(R_S \,||\, R_G)C_T}$$

where $C_T = C_{gs} + C_{in}(miller)$

This network is further reduced as follows since $R_s << R_G$

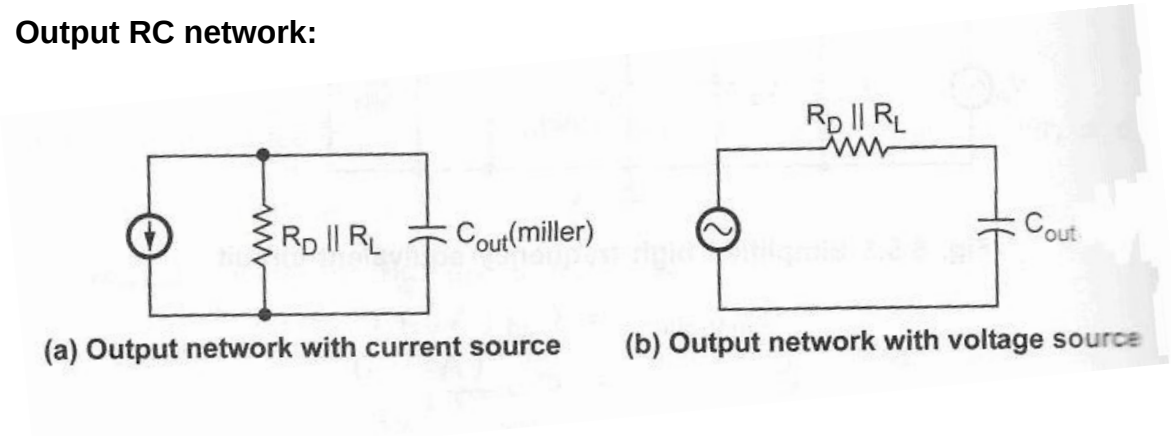
The critical frequency for the reduced input RC network is,

$$f_{c\,(input)} = \frac{1}{2\pi R_s C_T}$$

$$\text{or } f_c = \frac{1}{2\pi R_s [C_{gs} + C_{in\,(miller)}]}$$

The phase shift in high frequency RC network is $\theta = \tan^{-1}\left(\frac{R_s}{X_{C_T}}\right)$

Output RC network:



(a) Output network with current source (b) Output network with voltage source

The critical frequency for the above circuit is,

$$f_c = \frac{1}{2\pi R_o C_{out\,(miller)}} = \frac{1}{2\pi (R_D \parallel R_L) C_{out\,(miller)}}$$

It is not necessary that these frequencies should be equal. The network which has lower critical frequency than other network is called dominant pole

The phase shift in high frequency is

$$\theta = \tan^{-1}\left(\frac{R_o}{X_{C\,out\,(Miller)}}\right)$$

Unit-V

IC MOSFET Amplifiers

Part – A

1. Define an Integrated circuit. [CO5-L1]

An integrated circuit(IC) is a miniature ,low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon.The active components are transistors and diodes and passive components are resistors and capacitors.

2. What are the advantages of ICs over discrete circuits.? [CO5-L2]

- Minimization & hence increased equipment density.
- Cost reduction due to batch processing.
- Increased system reliability
- Improved functional performance.
- Matched devices.
- Increased operating speeds
- Reduction in power consumption

3. List the disadvantages of ICs [CO5-L1]

- Inductors cannot be fabricated
- IC function at very low voltage
- Limited amount of power
- Excessive heat

4. Define steering current. (May/June 2007) [CO5-L43

In integrated circuit designs circuits use constant sources.here the constant d.c current called reference current is generated at one location and is then replicated at various other locations for biasing the various stages of amplifier present in the circuit. this process is known as current steering.

5. State the advantages of current steering? (Nov/Dec 2006) [CO5-L4]

- The external components such as precision resistors required to generate a predictable and stable reference current,need not be repeated for every amplifier stage.
- The bias currents of the various stages track each other when there is any change due to power supply voltage or temperature.

6. Define cascade current mirror circuit. (May/Jun 2010) [CO5-L1]

MOSFET current source circuits the output resistance is a measure of stability of Io with respect to the changes in the output voltage. Here MOSFET T3 andT4 are included to provide higher output resistance. This circuit is known as cascade current mirror circuit.

7. Define Wilson current mirror circuit? (Nov/Dec 2008) [CO5-L3]

MOSFET Wilson current source the VDS values of T1 and T2 are not equal. Since λ is not zero, the ratio Io/Iref is slightly different from the aspect ratio.

8. State the advantages of Wilson current mirror circuit. [CO5-L2]

The advantages of these circuits are the increase in output resistance and hence increase the stability of output current.

9. List the various types of active loads? [CO5-L3]

There are three types of load devices:

- N-channel enhancement mode device
- N-channel depletion-mode device
- P-channel enhancement mode device

10. State the advantages of NMOS amplifier with depletion load over enhancement load. [CO5-L2]

The voltage gain of NMOS amplifier with depletion load is significantly larger than that with the enhancement load, however, like NMOS amplifier with enhancement load, the body effect lowers the small-signal voltage gain.

11. Define β and α. (May/Jun 2010) [CO5-L1]

- α is a current gain which is the ratio of collector current to the base current.
- β is a forward current gain which is the ratio of collector current to the emitter current.

12. What is meant by over drive factor? [CO5-L1]

The over drive factor is defined as the ratio of I_B and I_{BS}. Where, I_B is the base current and I_{BS} is the base current that produces the saturation.

13. Define delay time. [CO5-L3]

During the delay time period, base emitter voltage V_{BE} is applied, the base current I_B rises to I_{BS} and the collector current I_C is equal to zero or collector emitter leakage current I_{CEO}. The time required to charge the base emitter capacitance to, V_{BES}=0.7 V.

14. Define rise time. (May/June 2010) [CO5-L2]

During the rise time period, collector current I_C raises to steady state values I_{CS} and the collector emitter voltage falls from V_{CC} to V_{CES} the rise time depends on the input capacitance.

15. What is the need of driver circuit? [CO5-L2]

- It provides amplified voltage and current to the device.
- It provides isolation between control circuit and power circuit.

16. State methods which are used to provide effect of increased R_E. [CO5-L3]

- Constant current bias method
- Use of current mirror circuit
- Use of an active load.

17. What is current mirror? Dec-04 [CO5-L2]

The circuit in which the output current is forced to equal the input current is called as current mirror circuit. In a current mirror circuit, the output current is the mirror image of input current.

18. State advantages of current mirror circuit. [CO5-L3]

- Provides very high emitter resistance R_E.
- Easy to fabricate.
- Requires less components then constants current bias.
- Simple to design
- With properly matched transistors, collector current thermal stability is achieved.

19. What are the types of internal capacitance in the MOSFET? [CO5-L1]

There two types of

- Gate capacitance
- junction capacitance

20. Define gate capacitance. [CO5-L1]

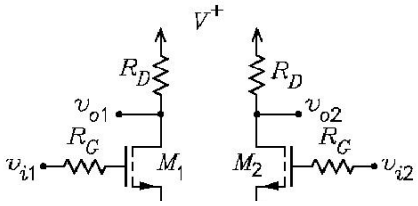
It is a parallel plate capacitance formed by a gate electrode with the channel with the oxide layer acts as a capacitor dielectric. It is denoted as Cox.

21. List the advantage of active load. [CO5-L2]

- provides very high ac resistance
- provides high differential mode voltage gain
- Ad High
- CMRR High

Part- B

1. Explain in detail about MOSFET Differential amplifier. [CO5-H1]



to solve for $\sqrt{I_D}$, then square the result to obtain

$$I_D = \left(\frac{-b + \sqrt{b^2 - 4ac}}{2a} \right)^2$$

Note that there is a second solution using the minus sign for the radical. This solution results in $V_{GS} < V_{TO}$, which is a non realizable solution. The desired solution is the one which gives the smaller value of I_D.

DC

(e) Check for the active mode. For the active mode, $V_{DS} > V_{GS} - V_{TO} = \sqrt{I_D/K}$.

(a) Ze

$$V_{DS} = V_D - V_S = (V_{DD} - I_D R_{DD}) - V_S = (V_{DD} - I_D R_{DD}) - \left(\sqrt{\frac{I_D}{K}} - V_{TO} \right)$$

$I'_Q/2$ i

The ci

2. Thi

(f) If $R_Q = \infty$, it follows that $I_{D1} = I_{D2} = I'_Q/2$.

(e)

bias n

Small-Signal or AC Solutions

The solutions assume that the two FETs are matched.

(f) (a) Calculate g_m and r_s.

$$g_m = 2\sqrt{K I_D} \qquad r_s = \frac{1}{g_m}$$

(b) Redraw the circuit with $V^+ = V^- = 0$ and $I'_Q = 0$. Replace the two FETs with the simple T model. The source part of the circuit obtained is shown in 3.

(c) Solve for i'_{s1} and i'_{s2}.

$$i'_{s1} = \frac{v_{i1}}{r_s + R_S + R_Q \| (r_s + R_S)} - \frac{v_{i2}}{r_s + R_S + R_Q \| (r_s + R_S)} \frac{R_Q}{R_Q + r_s + R_S}$$

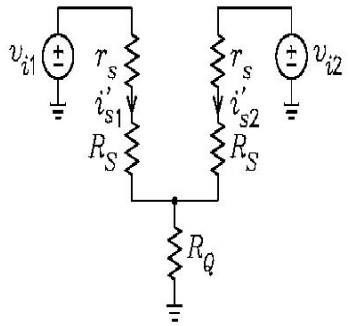


Figure 3: Source equivalent circuit for $r_0 = \infty$.

$$v_{o1} = -i'_{d1} r_{id} \| R_D = -i'_{s1} r_{id} \| R_D = \frac{-r_{id} \| R_D}{r_s + R_S + R_Q \| (r_s + R_S)} \left(v_{i1} - v_{i2} \frac{R_Q}{R_Q + r_s + R_S} \right)$$

$$v_{o2} = -i'_{d2} r_{id} \| R_D = -i'_{s1} r_{id} \| R_D = \frac{-r_{id} \| R_D}{r_s + R_S + R_Q \| (r_s + R_S)} \left(v_{i2} - v_{i1} \frac{R_Q}{R_Q + r_s + R_S} \right)$$

$$r_{out1} = r_{out2} = r_{id} \| R_D$$

(e) Special case for $R_Q = \infty$.

$$v_{o1} = \frac{-r_{id} \| R_D}{2 (r_s + R_S)} (v_{i1} - v_{i2}) \qquad v_{o2} = \frac{-r_{id} \| R_D}{2 (r_s + R_S)} (v_{i2} - v_{i1})$$

(f) To include the body effect in these equations, divide all input voltages by $1 + \chi$ and replace r_s with $r'_s = r_s / (1 + \chi)$, where $\chi = g_{mb}/g_m$ is the transconductance ratio. If $R_S = 0$ and $R_Q = \infty$, the factor $1 + \chi$ cancels out in the equations for v_{o1} and v_{o2} and the body effect goes away.

Common-Mode Rejection Ratio

The $CMRR$ for the BJT differential amplifier was defined with the output taken from only one side of the diff amp. To illustrate another way of defining the $CMRR$, it will be assumed that the output is taken differentially between the two outputs. In this case, the $CMRR$ is doubled.

(a) Define the differential input and output voltages

$$v_{id} = v_{i1} - v_{i2} \qquad v_{od} = v_{o1} - v_{o2}$$

(b) With $v_{i1} = v_{id}/2$ and $v_{i2} = -v_{id}/2$, use the solutions from above to solve for the differential output voltage v_{od}.

$$\begin{aligned} v_{od} &= v_{o1} - v_{o2} = \frac{-r_{id} \| R_D}{r_s + R_S + R_Q \| (r_s + R_S)} \left(1 + \frac{R_Q}{R_Q + r_s + R_S} \right) \frac{v_{id}}{2} \\ &= \frac{-r_{id} \| R_D}{r_s + R_S + R_Q \| (r_s + R_S)} \frac{2R_Q + r_s + R_S}{R_Q + r_s + R_S} \frac{v_{id}}{2} \end{aligned}$$

Solve for the differential gain A_v.

$$A_{vd} = \frac{v_{od}}{v_{id}} = \frac{1}{2} \frac{-r_{id} \| R_D}{r_s + R_S + R_Q \| (r_s + R_S)} \frac{2R_Q + r_s + R_S}{R_Q + r_s + R_S}$$

(c) Define the common-mode input and output voltages v_{icm} and v_{ocm}.

$$v_{icm} = \frac{v_{i1} + v_{i2}}{2} \qquad v_{ocm} = \frac{v_{o1} + v_{o2}}{2}$$

(d) With $v_{i1} = v_{i2} = v_{icm}$, use the solutions from above to solve for the common-mode output voltage v_{ocm}.

$$\begin{aligned} v_{ocm} &= \frac{v_{o1} + v_{o2}}{2} = \frac{1}{2} \frac{-r_{id} \| R_D}{r_s + R_S + R_Q \| (r_s + R_S)} \left(1 - \frac{R_Q}{R_Q + r_s + R_S}\right) v_{icm} \\ &= \frac{1}{2} \frac{-r_{id} \| R_D}{r_s + R_S + R_Q \| (r_s + R_S)} \frac{r_s + R_S}{R_Q + r_s + R_S} v_{icm} \end{aligned}$$

Solve for the common-mode voltage gain A_{vcm}.

$$A_{vcm} = \frac{v_{ocm}}{v_{icm}} = \frac{1}{2} \frac{-r_{id} \| R_D}{r_s + R_S + R_Q \| (r_s + R_S)} \frac{r_s + R_S}{R_Q + r_s + R_S}$$

(e) Solve for the common-mode rejection ratio.

$$CMRR = \left| \frac{A_{vd}}{A_{vcm}} \right| = \frac{2R_Q + r_s + R_S}{r_s + R_S} = 1 + \frac{2R_Q}{r_s + R_S}$$

Express this in dB.

$$CMRR_{dB} = 20 \log \left(1 + \frac{2R_Q}{r_s + R_S}\right)$$

(f) To include the body effect in the equation for $CMRR$, replace r_s with $r_s' = r_s / (1 + \chi)$.

2. Find the CMRR for the circuit with given data. [CO5-H2]

Example 1 *For* $I_Q = 2\,\text{mA}$, $R_Q = 50\,\text{k}\Omega$, $R_G = 1\,\text{k}\Omega$, $R_S = 100\,\Omega$, $R_D = 10\,\text{k}\Omega$, $V^+ = 20\,\text{V}$, $V^- = -20\,\text{V}$, $K = 2.5 \times 10^{-3}\,\text{A/V}^2$, $V_{TO} = 1.5\,\text{V}$, *and* $\lambda = 0.01$, *calculate* v_{o1}, v_{o2}, v_{od}, r_{out}, *and* $CMRR$.

Solution.

$$I_{D1} = I_{D2} = \frac{I_Q}{2} = 1\,\text{mA} \qquad V_{GS} = V_{TO} + \sqrt{\frac{I_D}{K}} = 2.132\,\text{V}$$

$$V_{DS} = V_D - V_S = \left(V^+ - \frac{I_Q}{2}R_D\right) - (-V_{GS}) = 12.13\,\text{V}$$

$$g_m = 2\sqrt{KI_D} = 3.162\,\text{mS} \qquad r_s = \frac{1}{g_m} = 316.23\,\Omega \qquad r_0 = \frac{\lambda^{-1} + V_{DS}}{I_D} = 112.1\,\text{k}\Omega$$

$$R_{ts} = R_S + R_Q \| (r_s + R_S) = 512.79\,\Omega \qquad r_{id} = r_0\left(1 + \frac{R_{ts}}{r_s}\right) + R_{ts} = 294.5\,\text{k}\Omega$$

$$v_{o1} = \frac{-r_{id}\|R_D}{r_s + R_S + R_Q\|(r_s + R_S)}\left(v_{i1} - v_{i2}\frac{R_Q}{R_Q + r_s + R_S}\right) = -11.67v_{i1} + 11.57v_{i2}$$

$$v_{o2} = -11.67v_{i2} + 11.57v_{i1}$$

$$v_{od} = v_{o1} - v_{o2} = -23.24\,(v_{i1} - v_{i2}) \qquad r_{out} = r_{id}\|R_D = 9.672\,\text{k}\Omega$$

$$v_{ocm} = \frac{v_{o1} + v_{o2}}{2} = -0.096v_{icm}$$

$$A_{vd} = \frac{-r_{id}\|R_D}{r_s + R_S + R_Q\|(r_s + R_S)}\frac{2R_Q + r_s + R_S}{R_Q + r_s + R_S} = -23.24$$

$$A_{vcm} = \frac{-r_{id}\|R_D}{r_s + R_S + R_Q\|(r_s + R_S)}\frac{r_s + R_S}{R_Q + r_s + R_S} = -0.096$$

$$CMRR_{dB} = 20\log\left|\frac{A_{vd}}{A_{vcm}}\right| = 47.65\,\text{dB}$$