SKP Engineering College

Tiruvannamalai – 606611

A Course Material

on

Electronic Devices

By

K.Vijayalakshmi

Assistant Professor

Electronics and Communication Engineering Department

Quality Certificate

This is to Certify that the Electronic Study Material

Subject Code: EC6201

Subject Name: Electronic Devices

Year/Sem: I/II

Being prepared by me and it meets the knowledge requirement of the University curriculum.

Signature of the Author

Name: K.Vijayalakshmi

Designation: Assistant Professor

This is to certify that the course material being prepared by Ms. K.Vijayalakshmi is of the adequate quality. He has referred more than five books and one among them is from abroad author.

Signature of HD

Name:

Seal:

Signature of the Principal

Name: Dr.V.Subramania Bharathi

Seal:

EC6201 ELECTRONIC DEVICES LTPC 3 0 0 3

OBJECTIVES: The student should be made to:

- Be exposed to basic electronic devices
- Be familiar with the theory, construction, and operation of Basic electronic devices.

UNIT I SEMICONDUCTOR DIODE 9

PN junction diode, Current equations, Diffusion and drift current densities, forward and reverse bias characteristics, Switching Characteristics.

UNIT II BIPOLAR JUNCTION 9

NPN -PNP -Junctions-Early effect-Current equations – Input and Output characteristics of CE, CB CC-Hybrid -π model - h-parameter model, Ebers Moll Model-Gummel Poon-model, Multi Emitter Transistor.

UNIT III FIELD EFFECT TRANSISTORS 9

JFETs – Drain and Transfer characteristics,-Current equations-Pinch off voltage and its significance- MOSFET- Characteristics- Threshold voltage -Channel length modulation, D-MOSFET, E-MOSFET-, Current equation - Equivalent circuit model and its parameters, FINFET,DUAL GATE MOSFET.

UNIT IV SPECIAL SEMICONDUCTOR DEVICES 9

Metal-Semiconductor Junction- MESFET, Schottky barrier diode-Zener diode-Varactor diode –Tunnel diode- Gallium Arsenide device, LASER diode, LDR.

UNIT V POWER DEVICES AND DISPLAY DEVICES 9

UJT, SCR, Diac, Triac, Power BJT- Power MOSFET- DMOS-VMOS. LED, LCD, Photo transistor, Opto Coupler, Solar cell, CCD.

TOTAL PERIODS: 45

OUTCOMES: At the end of the course, the student should be able to:

- Explain the theory, construction, and operation of basic electronic devices.
- Use the basic electronic devices

TEXT BOOKS

1. Donald A Neaman, "Semiconductor Physics and Devices", Third Edition, Tata Mc GrawHill Inc. 2007.

REFERENCES:

1. Yang, "Fundamentals of Semiconductor devices", McGraw Hill International Edition, 1978.
2. Robert Boylestad and Louis Nashelsky, "Electron Devices and Circuit Theory" Pearson Prentice Hall, 10th edition,July 2008.

CONTENTS

S.No	Particulars	Page
1	Unit – I	5
2	Unit – II	28
3	Unit – III	54
4	Unit – IV	78
5	Unit – V	102

Unit - I

Semiconductor Diode

Part - A

1. What are semiconductors?

The materials whose electrical property lies between those of conductors and insulators are known as Semiconductors. Ex germanium, silicon.

It has two types.

1. Intrinsic semiconductor 2. Extrinsic semiconductor.

2. Differentiate between intrinsic and extrinsic semiconductor [CO1– L2 - May/June 2014]

Pure form of semiconductors are said to be intrinsic semiconductor.

Ex: germanium, silicon.

It has poor conductivity

If certain amount of impurity atom is added to intrinsic semiconductor the resulting semiconductor is Extrinsic or impure Semiconductor

It has good conductivity.

3. Define drift current? [CO1 – L1 - May/June 2012]

When an electric field is applied across the semiconductor, the holes move towards the negative terminal of the battery and electron move towards the positive terminal of the battery. This drift movement of charge carriers will result in a current termed as drift current.

4. Give the expression for drift current density [CO1– L2 - Nov/Dec 2013]

Drift current density due to electrons

$$J_n = q\, n\, \mu_n E$$

Where,

J_n - drift current density due to electron q- Charge of electron

μ_n - Mobility of electron E - applied electric field

Drift current density due to holes**.**

$$J_p = q\, p\, \mu_p E$$

Where,

J_n - drift current density due to holes q - Charge of holes

μ_p - Mobility of holes E - applied electric field

5. Define the term diffusion current? [CO1 – L1 - May/June 2011]

A concentration gradient exists, if the number of either electrons or holes is greater in one region of a semiconductor as compared to the rest of the region. The holes and electron tend to move from region of higher concentration to the region of lower concentration. This process in called diffusion and the current produced due this movement is diffusion current.

6. Give the expression for diffusion current density[CO1 – L2 - May/June 2014]

Diffusion current density due to electrons

$$J_n = q\, D_n\, dn / dx$$

Where

Jn - diffusion current density due to electron q - Charge of an electron

Dn – diffusion constant for electron dn / dx – concentration gradient

Diffusion current density due to holes

$$Jp = - q\ Dp\ dp / dx$$

Where

Jp - diffusion current density due to holes q - Charge of a hole

Dp – diffusion constant for hole dn / dx – concentration gradient

7. Differentiate between drift and diffusion currents. [CO1 – L2 - Nov/Dec 2014]

Drift current

1. It is developed due to potential gradient.

2. This phenomenon is found both in metals and semiconductors

Diffusion current

1. It is developed due to charge concentration gradient.

2. This phenomenon is found only in metals

8. What is depletion region in PN junction? [CO1 – L1 - May/June 2013]

The region around the junction from which the mobile charge carriers (electrons and holes) are depleted is called as depletion region. since this region has immobile ions, which are electrically charged , the depletion region is also known as space charge region.

9. What is barrier potential? [CO1 –L1]

Because of the oppositely charged ions present on both sides of PN junction an electric potential is established across the junction even without any external voltage source which is termed as barrier potential.

10. What is Reverse saturation current? [CO1 – L1 - May/June 2011]

The current due to the minority carriers in reverse bias is said to be reverse saturation current. This current is independent of the value of the reverse bias voltage.

11. What is the total current at the junction of pn junction diode? [CO1 – L2 - May/June 2015]

The total in the junction is due to the hole current entering the n material and theelectron current entering the p material. Total current is given by

$$I = I_{pn}(0) + I_{np}(0)$$

Where,

I – Total current

Ipn(0) - hole current entering the n material

Inp(0) - electron current entering the p material

12. Give the diode current equation? [CO1 – L1 - May/June 2015]

The diode current equation relating the voltage V and current I is given by

$I = I_0\left[e^{(v/\eta vT}\right) - 1$

where

I – diode current

I_o – diode reverse saturation current at room temperature

V – External voltage applied to the diode η - a constant, 1 for Ge and 2 for Si

V_T = kT/q = T/11600, thermal voltage

K – Boltzmann's constant (1.38066x10^-23 J/K)

q – Charge of electron (1.6x10^-19 C)

T – Temperature of the diode junction

13. What is recovery time? Give its types. [CO1 – L2 - Nov/Dec 2013]

When a diode has its state changed from one type of bias to other a transient accompanies the diode response, i.e., the diode reaches steady state only after an interval of time " tr" called as recovery time. The recovery time can be divided in to two types such as

(i) forward recovery time

(ii) reverse recovery time

14. Define storage time. [CO1 – L1]

The interval time for the stored minority charge to become zero is called storage time. It is represented as t_s.

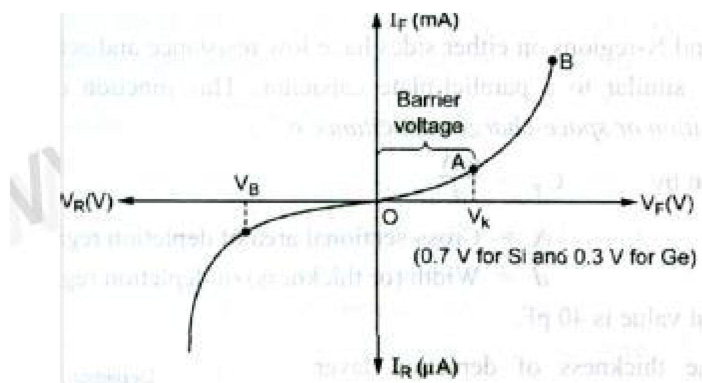
15. Define transition time. [CO1 – L1]

The time when the diode has normally recovered and the diode reverse current reaches reverse saturation current Io is called as transition time. It is represented as t_t

16. Define PIV. [CO1 – L1]

Peak inverse voltage is the maximum reverse voltage that can be applied to the PN junction without damage to the junction.

17. Draw V-I characteristics of pn diode[CO1 – L2 - May/June 2014]



18. Write the application of PN diode [CO1 – L3 - Nov/Dec 2014]

Can be used as rectifier in DC Power Supplies.

- In Demodulation or Detector Circuits.
- In clamping networks used as DC Restorers
- In clipping circuits used for waveform generation.
- As switches in digital logic circuits.
- In demodulation circuits.

PART B

1. Explain the drift and diffusion currents for PN diode. [CO1 – L2 - May/June 2014] [8]

Drift and Diffusion Currents:

The flow of charge (ie) current through a semiconductor material are of two types namely drift & diffusion.

(ie) The net current that flows through a (PN junction diode) semiconductor material has two components

Drift current

Drift Current:

→ When an electric field is applied across the semiconductor material, the charge carriers attain a certain drift velocity V_d , which is equal to the product of the mobility of the charge carriers and the applied Electric Field intensity E ;

Drift velocity V_d = mobility of the charge carriers X Applied Electric field intensity

→ Holes move towards the negative terminal of the battery and electrons move towards the positive terminal of the battery. This combined effect of movement of the charge carriers constitutes a current known as — the drift current — .

→ Thus the drift current is defined as the flow of electric current due to the motion of the charge carriers under the influence of an external electric field.

→ Drift current due to the charge carriers such as free electrons and holes are the current passing through a square centimeter perpendicular to the direction of flow.

(i) Drift current density J_n , due to free electrons is given

by

$$J_n = q\, n\, \mu_n\, E\ A / cm^2$$

(ii) Drift current density J_P, $_2$due to holes is given by

$$J_P = q\, p\, \mu_p\, E\ A / cm$$

Where, n - Number of free electrons per cubic centimeter.

P - Number of holes per cubic centimeter

μ_n – Mobility of electrons in cm^2 / Vs

μ_p – Mobility of holes in cm^2 / Vs

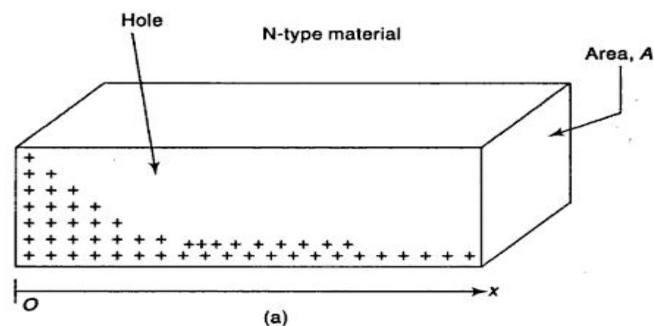
E – Applied Electric filed Intensity in V /cm

q – Charge of an electron = 1.6 x 10^{-19} coulomb.

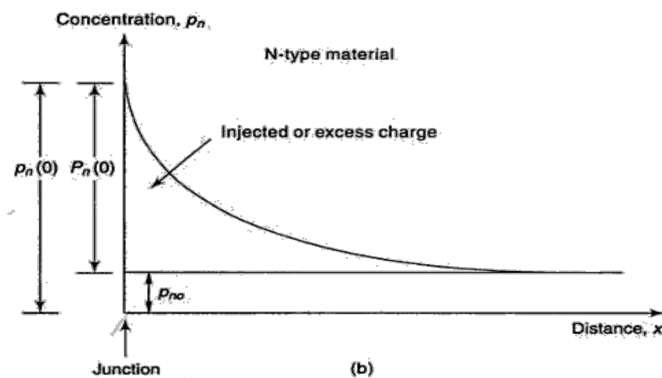
Diffusion Current:

→ It is possible for an electric current to flow in a semiconductor even in the absence of the applied voltage provided a concentration gradient exists in the material.

→ A concentration gradient exists if the number of either elements or holes is greater in one region of a semiconductor as compared to the rest of the Region.



(a)



(a) Exess hole concentration varying along the axis in an N-type semiconductor bar

(b) The resulting diffusion current

→ In a semiconductor material the change carriers have the tendency to move from the

region of higher concentration to that of lower concentration of the same type of charge carriers. Thus the movement of charge carriers takes place resulting in a current called diffusion current.

As indicated in fig a, the hole concentration p(x) in semiconductor bar varies from a high value to a low value along the x-axis and is constant in the y and z directions.

Diffusion current density due to holes J_p is given by

$$J_p = -qD_p \frac{dp}{dx} \ A/cm^2$$

Since the hole density p(x) decreases with increasing x as shown in fig b, dp/dx is negative and the minus sign in equation is needed in order that J_p has positive sign in the positive x direction.

Diffusion current density due to the free electrons is given by

Where dn/dx – concentration gradient for electrons

Dp/dx - concentration gradient for holes

$$J_n = qD_n \frac{dn}{dx} \ A/cm^2$$

D_n and D_p – diffusion coefficient for electrons and holes

Total Current:

The total current in a semiconductor is the sum of both drift and diffusion currents that is given by

$$J_p = qP\mu_p E - qD_p \frac{dp}{dx}$$

Similarly the total current density for an N type semiconductor is given by

$$J_n = qn\mu_n E - qD_n \frac{dn}{dx}$$

2. Derive the PN diode current equation.[CO1 – L2 - May/June 2015] [6]

Diode Current Equation:

The diode current equation relating the voltage V and current I is given by

where

I – diode current

I_o – diode reverse saturation current at room temperature V – external voltage applied to the diode

Ƞ - a constant, 1 for Ge and 2 for Si V_T = kT/q = T/11600, thermal voltage

K – Boltzmann‘s constant (1.38066x10^-23 J/K) q – charge of electron (1.6x10^-19 C)

T – temperature of the diode junction

At room temperature (T=300 K), V_T = 26mV. Substituting this value in current equation,

$I = I_0[e^{\frac{40v}{\eta}} - 1]$

For germanium diode,

$I = I_0[e^{40v} - 1]$ since η=1 for Ge

For silicon diode,

$I = I_0[e^{20v} - 1]$ since η=1 for si

If the value of applied voltage is greater than unity, then the equation of diode current for germanium, $I_0[e^{40v}]$

and for silicon,

$I_0[e^{20v}]$

when the diode is reverse biased, its current equation may be obtained by changing the sign of voltage V. Thus diode current with reverse bias is

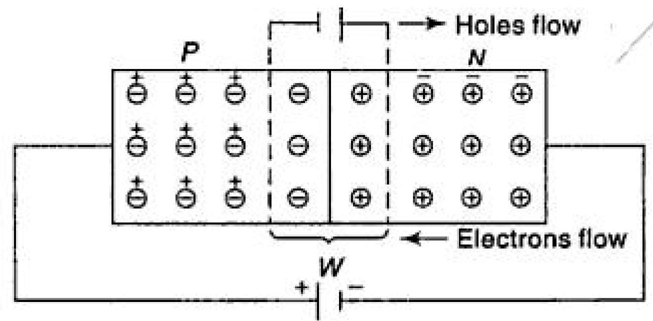
$I = I_0\left[e^{(-v/}\eta\mathrm{vT}\right) - 1$

3. Explain the operation of PN junction under forward bias condition with its characteristics. [CO1 – L2 - May/June 2014] [8]

Forward Bias Condition:

When positive terminal of the battery is connected to the P-type and negative terminal to N-type of the PN junction diode that is known as forward bias condition.

Operation



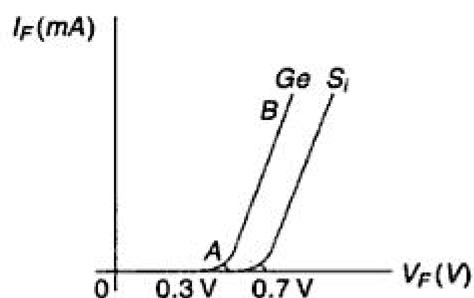
The applied potential in external battery acts in opposition to the internal potential barrier which disturbs the equilibrium.

As soon as equilibrium is disturbed by the application of an external voltage, the Fermi level is no longer continuous across the junction.

Under the forward bias condition the applied positive potential repels the holes in P type region so that the holes move towards the junction and the applied positive potential repels the electrons in N type region so that the electrons move towards the junction.

When the applied potential is more than the internal barrier potential the depletion region and internal potential barrier disappear.

V-I Characteristics



As the forward voltage increased for V_F < Vo, the forward current I_F almost zero because the potential barrier prevents the holes from P region and electrons from N region to flow across the depletion region in opposite direction.

For V_F > Vo, the potential barrier at the junction completely disappears and hence, the holes cross the junction from P to N type and electrons cross the junction to opposite direction, resulting

large current flow in external circuit.

A feature noted here is the cut in voltage or threshold voltage V_F below which the current is very small.

At this voltage the potential barrier is overcome and the current through the junction starts to increase rapidly.

Cut in voltage is 0.3V for germanium and 0.7 for silicon.

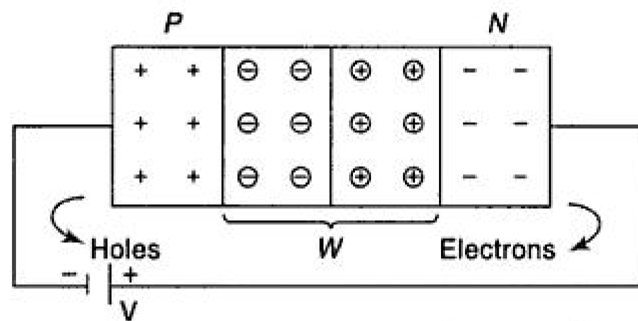
4. Explain the operation of PN junction under reverse bias condition with its Characteristics. [CO1 – L2 - May/June 2012] (8)

Under Reverse Bias Condition:

When the negative terminal of the battery is connected to the P-type and positive terminal to N-type of the PN junction diode that is known as forward bias condition.

Operation

The holes from the majority carriers of the P side move towards the negative terminal of the battery and electrons which from the majority carrier of the N side are attracted towards the positive terminal of the battery.



Hence, the width of the depletion region which is depleted of mobile charge carriers increases. Thus, the electric field produced by applied reverse bias, is in the same direction as the electric field of the potential barrier.

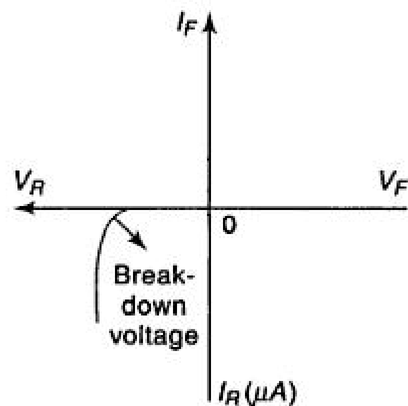
Hence the resultant potential barrier is increased which prevents the flow of majority carriers in both directions. The depletion width W is proportional to under reverse bias.

V-I characteristics

Theoretically no current flow in the external circuit. But in practice a very small amount of current of the order of few microamperes flows under reverse bias.

Electrons forming covalent bonds of semiconductor atoms in the P and N type regions may absorb sufficient energy from heat and light to cause breaking covalent bonds. So electron hole pairs continuously produced.

Consequently the minority carriers electrons in the P region and holes in the N region, wander over to the junction and flow towards their majority carrier side giving rise a small reverse current. This current is known as reverse saturation current Io.



The magnitude of this current is depends on the temperature because minority carrier is thermally broken covalent bonds.

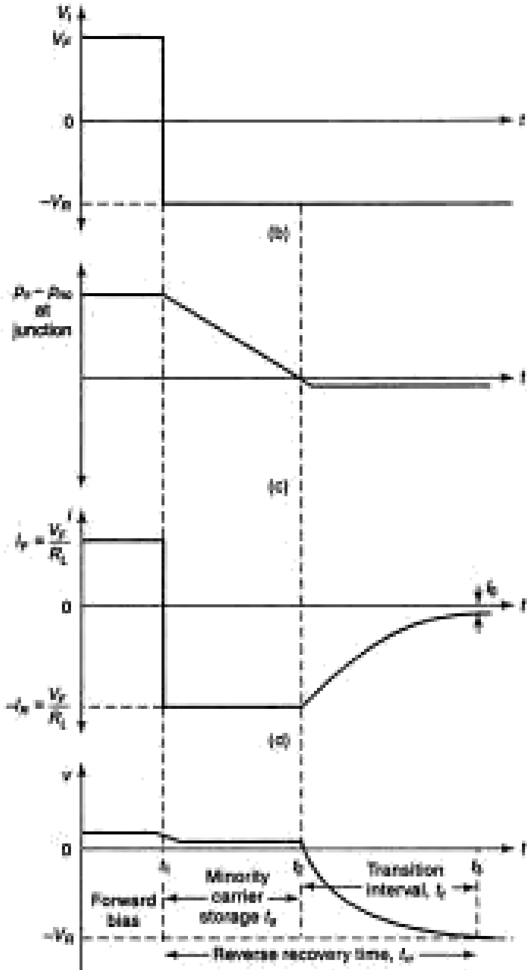
5. Explain details about the switching characteristics on PN diode with neat Sketch. [CO1 – L2 - May/June 2015] [12]

Diodes are often used in switching mode. When the applied bias voltage to the PN diode is suddenly reversed in opposite direction and it reaches a steady state at a interval of time that is called the recovery time.

Forward recovery time is defined is the time required the forward voltage or current to reach a specified value after switching diode from its reverse to forward biased state.

When PN diode is forward biased the minority electrons concentration in P region is linear. If the junction is suddenly reversed at t1 then because of stored electronic charge, the reverse current I_R is initially of the same magnitude as forward current I_F.

The diode will continue to conduct until the injected or excess minority carrier density (p-po) or (n-no) has dropped to zero shown in fig. c.



In fig. b the applied voltage Vi = V_F for the time up to t1 is in the direction to forward bias the diode. The resistance R_L is large so that the drop across R_L is large when compared to the drop across diode. Then the current is I= V_F / R_L = I_F.

At time t=t1 the input voltage is reversed to the value of $–V_R$ current does not become zero and the value is I= V_R / R_L = I_R shown in fig d..

During the time interval from t1 to t2 the injected minority carriers have remained stored and hence this interval is called the storage time (t1).

After the instant t=t2, the diode gradually recovers and ultimately reaches the steady state. The time interval between t2 and instant t3 when the diode has recovered nominally is called the transition time t_t.

The recovery said to have completed (i) when even the minority carriers remote from the junction have difference to the junction and crossed it. (ii) when the junction transition capacitance C across the reverse biased junction has got charged through the external resistor R_L to the voltage $–V_R$.

For commercial switching type diodes the reverse recovery time t_{rr} ranges from less than 1ns up to as high as 1us.

In order to minimize the effect of reverse current the time period of the operating frequency should be a minimum of approximately 10 times t_{rr}. For example if diode has t_{rr} of 2ns its operating frequency is

The reverse recovery time can be reduced b shortening the length of the P region in a PN junction diode.

The stored storage and switching time can be reduced by introduction of gold impurities into junction diode by diffusion. The gold dopant also called a life time killer, increases the recombination rate and removes the stored minority carriers.

This technique is used to produce diodes and other active devices for high speed applications.

6. Explain the theory of PN Junction Diode. [CO1 – L2 - May/June 2012] [16]

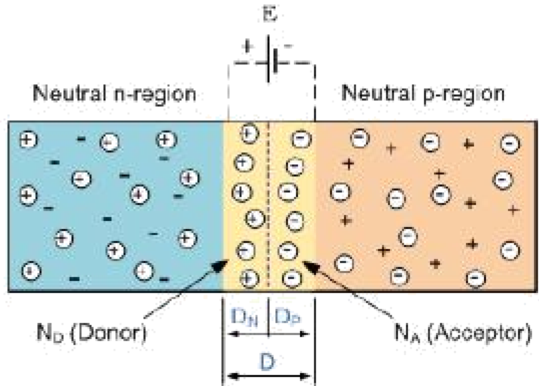
PN Junction:

When the N and P-type semiconductor materials are first joined together a very large density gradient exists between both sides of the junction so some of the free electrons from the donor impurity atoms begin to migrate across this newly formed junction to fill up the holes in the P-type material producing negative ions. However, because the electrons have moved across the junction from the N-type silicon to the P-type silicon, they leave behind positively charged donor ions (ND) on the negative side and now the holes from the acceptor impurity migrate across the junction in the opposite direction into the region are there are large numbers of free electrons. As a result, the charge density of the P-type along the junction is filled with negatively charged acceptor ions (NA), and the charge density of the N-type along the junction becomes positive. This charge transfer of electrons and holes across the junction is known as diffusion.

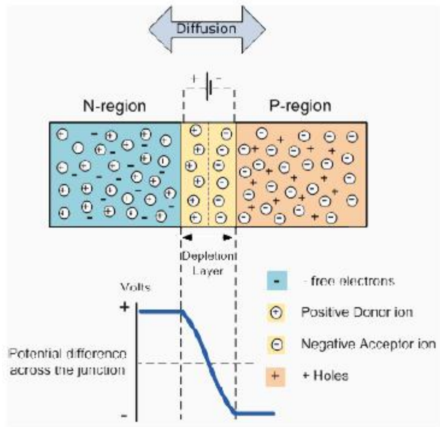
This process continues back and forth until the number of electrons which have crossed the junction have a large enough electrical charge to repel or prevent any more carriers from crossing the junction. The regions on both sides of the junction become depleted of any free carriers in comparison to the N and P type materials away from the junction. Eventually a state of equilibrium (electrically neutral situation) will occur producing a "potential barrier" zone around the area of the junction as the donor atoms repel the holes and the acceptor atoms repel the electrons. Since no free charge carriers can rest in a position where there is a potential barrier the regions on both sides

of the junction become depleted of any more free carriers in comparison to the N and P type materials away from the junction. This area around the junction is now called the Depletion Layer.

The Pn Junction



The total charge on each side of the junction must be equal and opposite to maintain a neutral charge condition around the junction. If the depletion layer region has a distance D, it therefore must therefore penetrate into the silicon by a distance of Dp for the positive side, and a distance of Dn for the negative side giving a relationship between the two of Dp.NA = Dn.ND in order to maintain charge neutrality also called equilibrium.



PN Junction Distance:

As the N-type material has lost electrons and the P-type has lost holes, the N-type material has become positive with respect to the P-type. Then the presence of impurity ions on both sides of the junction cause an electric field to be established across this region with the N-side at a positive voltage relative to the P-side. The problem now is that a free charge requires some extra energy to overcome the barrier that now exists for it to be able to cross the depletion region junction. This electric field created by the diffusion process has created a "built-in potential difference" across the junction with an open-circuit (zero bias) potential of:

$$E_0 = V_T \ln \left(N_D N_A / n_i^{\,2}\right.$$

Where: Eo is the zero bias junction voltage, VT the thermal voltage of 26mV at room temperature, ND and NA are the impurity concentrations and ni is the intrinsic concentration.

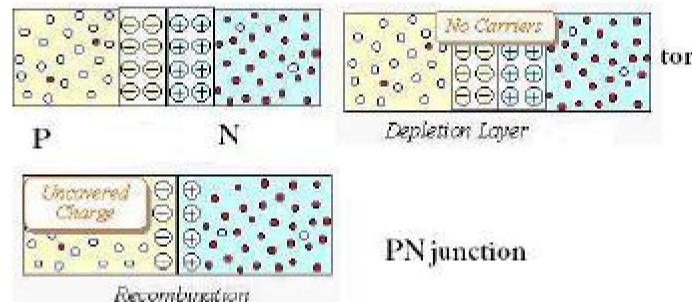
A suitable positive voltage (forward bias) applied between the two ends of the PN junction can supply the free electrons and holes with the extra energy. The external voltage required to overcome this potential barrier that now exists is very much dependent upon the type of semiconductor material used and its actual temperature. Typically at room temperature the voltage across the depletion layer for silicon is about 0.6 - 0.7 volts and for germanium is about 0.3 - 0.35 volts. This potential barrier will always exist even if the device is not connected to any external power source.

The significance of this built-in potential across the junction, is that it opposes both the flow of holes and electrons across the junction and is why it is called the potential barrier. In practice, a PN junction is formed within a single crystal of material rather than just simply joining or fusing together two separate pieces. Electrical contacts are also fused onto either side of the crystal to enable an electrical connection to be

made to an external circuit. Then the resulting device that has been made is called a PN junction Diode or Signal Diode.

Depletion Layer PN Junction:

If one side of crystal pure semiconductor Si(silicon) or Ge(Germanium) is doped with acceptor impurity atoms and the other side is doped with donor impurity atoms , a PN junction is formed as shown in figure.P region has high concentration of holes and N region contains large number of electrons.



As soon as the junction is formed, free electrons and holes cross through the junction by the process of diffusion.During this process , the electrons crossing the junction from N- region into P-region , recombine with holes in the P-region very close to the junction.Similarly holes crossing the junction from the P-region into the N-region, recombine with electrons in the N-region very close to the junction. Thus a region is formed, which does not have any mobile charge very close to the junction. This region is called the depletion layer of pn junction.

In this region, on the left side of the junction, the acceptor atoms become negative ions and on the right side of the junction, the donor atoms become positive ions as shown in figure.

Function Of Depletion Layer Of PN Junction:

An electric field is set up, between the donor and acceptor ions in the depletion layer of the pn junction .The potential at the N-side is higher than the potential at P-side.Therefore electrons in the N- side are prevented to go to the lower potential of P-side. Similarly, holes in the P-side find themselves at a lower potential and are prevented to cross to the N-side. Thus, there is a barrier at the junction which opposes the movement of the majority charge carriers. The difference of potential from one side of the barrier to the other side of the barrier is called potential barrier. The potential barrier is approximately 0.7V for a silicon PN junction and 0.3V for germanium PN junction. The distance from one side of the barrier to the other side is called the width of the barrier, which depends on the nature of the material.

Unit - II

Bipolar Junction

Part - A

1. Why an ordinary transistor is called bipolar? [CO2 – L2 - May/June 2012]

The operation of the transistor depends on both majority and minority carriers. So it is called bipolar device.

2. Collector region of transistor is larger than emitter. Why? [CO2 – L2 - May/June 2014]

Collector is made physically larger than emitter and base because collector is to dissipate much power.

3. Why is BJT is called current controlled device? [CO2 – L2 - Nov/Dec 2013]

The output voltage, current, or power is controlled by the input current in a transistor. So it is called the current controlled device.

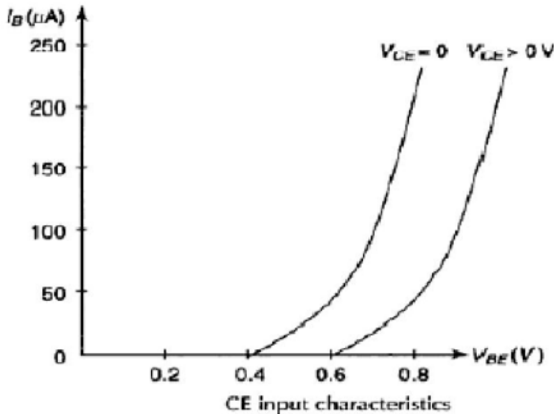
4. Define Early Effect. [CO2 – L1 - May/June 2015]

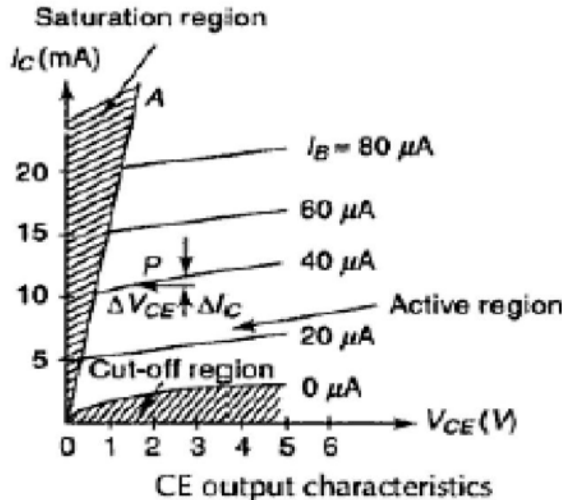
A variation of the base-collector voltage results in a variation of the quasi-neutral width in the base. The gradient of the minority-carrier density in the base therefore changes, yielding an increased collector current as the collector-base current is increased. This effect is referred to as the Early effect.

5. Among CE, CB, CC which one is most popular. Why? [CO2 – L2 - May/June 2012]

CE is most popular among the three because it has high gain compared to base and collector configuration. It has the gain about to 500 that finds excellent usage in audio frequency applications.

6. Draw the characteristics of CE configuration. [CO2 – L2 - May/June 2011]





7. Compare CE, CB, CC. [CO2 – L2 - May/June 2015]

Property	*CB*	*CE*	CC
Input resistance	Low (about 100 fl)	Moderate (about 750 Q)	High (about 750 *VS1)*
Output resistance	High (about 450 kQ)	Moderate (about 45 kfJ)	Low (about 25 O)
Current gain	I	High	High
Voltage gain	About 150	About 500	Less than 1
Phase shift between input & output voltages	0 or 360°	180°	0 or 360°
Applications	for high frequency circuits	for audio frequency circuits	for impedance matching

8. Why h parameter model is important for BJT [CO2 – L2 - May/June 2014]

It is important because:

1. its values are used on specification sheets
2. it is one model that may be used to analyze circuit behavior
3. it may be used to form the basis of a more accurate transistor model

9. Define current amplification factor [CO2 – L1 - May/June 2012]

In a transistor amplifier with a.c. input signal, the ratio of change in output current to be the change in input current is known as the current amplification factor.

In the CB configuration the current amplification factor, $\alpha = \frac{\Delta I_C}{\Delta I_E}$

In the CE configuration the current amplification factor, $\beta = \frac{\Delta I_C}{\Delta I_B}$

In the CC configuration the current amplification factor, $\gamma = \frac{\Delta I_E}{\Delta I_B}$

10. What do you meant by multi emitter transistor? [CO2 – L2 - May/June 2014]

Transistor–transistor logic (**TTL**) is a class of digital circuits built from bipolar junction transistors (BJT) and resistors. It is called *transistor–transistor logic* because both the logic gating function (e.g., AND) and the amplifying function are performed by transistors.

TTL is notable for being a widespread integrated circuit (IC) family used in many applications such as computers, industrial controls, test equipment and instrumentation, consumer electronics, synthesizers, etc.

11. In a CR connection, the value of I_E is 6.28 mA and the collector current Ic is 6.20 mA. Determine d.c. current gain. [CO2 – L3 - May/June 2013]

I_E = 6.28mA and Ic =6.20mA

We know that common base dc current gain

$$\alpha = \frac{I_C}{I_E}$$

$$= \frac{6.20 * 10^{-3}}{6.28 * 10^{-3}} = 0.987$$

12. The transistor has I_E = 10 mA and α = 0.98. Find the value of base and collector currents. [CO2 – L3 - Nov/Dec2012]

I_E=10mA and α=0.98

The common base dc current gain,

$$\alpha = \frac{I_C}{I_E}$$

$$0.98 = \frac{I_C}{10}$$

$$I_C = 0.98 * 10 = 9.8mA$$

The Emitter current $I_E=I_B+I_C$

$$10 = I_B + I_C$$

$$10 = I_B + 9.8$$

$$I_B = 0.2mA$$

13. If a transistor has a α of 0.97 find the value of β. If β=200, find the value of α. [CO2 – L3 - May/June 2015]

If

$$\alpha = 0.97, \beta = \frac{\alpha}{1-\alpha} = \frac{0.97}{1-0.97} = 32.33$$

If $\beta = 200, \alpha = \frac{\beta}{1+\beta} = \frac{200}{1+200} = 0.995$

14. Give some applications of BJT. [CO2 – L3 - May/June 2012]

The BJT remains a device that excels in some applications, such as discrete circuit design, due to the very wide selection of BJT types available, and because of its high transconductance and output resistance compared to MOSFETs.

The BJT is also the choice for demanding analog circuits, especially for very-high-frequency applications, such as radio-frequency circuits for wireless systems.

Bipolar transistors can be combined with MOSFETs in an integrated circuit by using a BICMOS process of wafer fabrication to create circuits that take advantage of the application strengths of both types of transistor.

PART B

1. Explain the operation of NPN and PNP transistors [CO2 – L2 - May/June 2014] [8]

Transistor Operation: The basic operation will be described using the pnp transistor. The operation of the pnp transistor is exactly the same if the roles played by the electron and hole are interchanged.

- One p-n junction of a transistor is reverse-biased, whereas the other is forward-biased

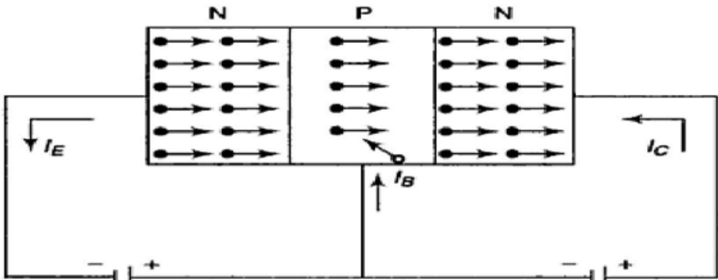


Fig. 6.4 Current in NPN transistor

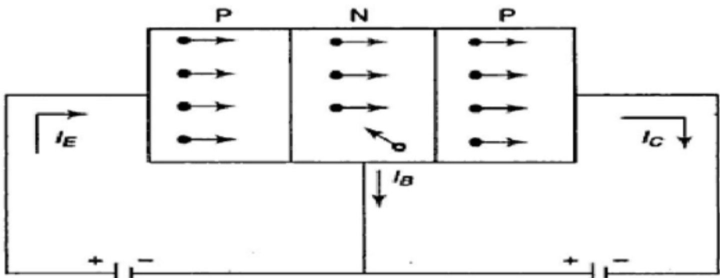


Fig. 6.5 Current in PNP transistor

- Both biasing potentials have been applied to a pnp transistor and resulting majority and Minority carrier flows indicated.

• Majority carriers (+) will diffuse across the forward-biased p-n junction into the n-type Material.

• A very small number of carriers (+) will through n-type material to the base terminal. Resulting IB is typically in order of microamperes.

• The large number of majority carriers will diffuse across the reverse-biased junction into the p-type material connected to the collector terminal.

• Majority carriers can cross the reverse-biased junction because the injected majority carriers will appear as minority carriers in the n-type material.

- Applying KCL to the transistor :

$$I_E = I_C + I_B$$

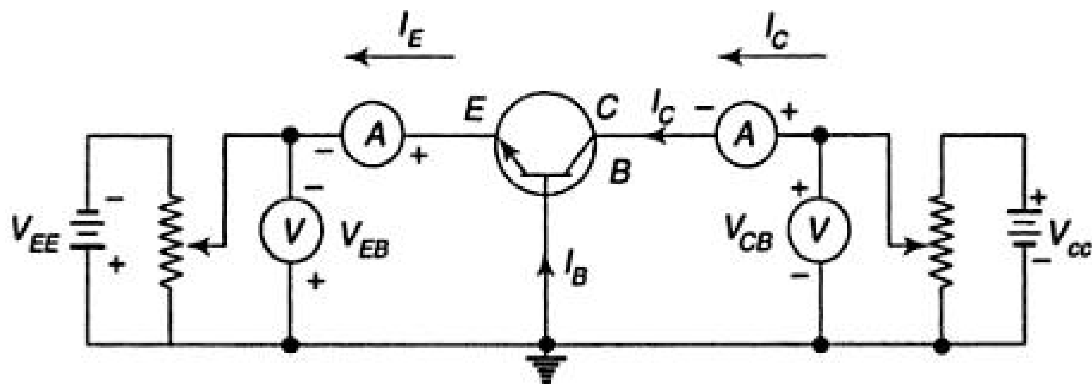
• The comprises of two components – the majority and minority carriers

$$I_C = I\ \text{majority} + I_{CO}\text{minority}$$

• I_{CO} – I_C current with emitter terminal open and is called leakage current.

2. Explain the input and output characteristics of a transistor in CB configuration. [CO2 – L2 - May/June 2012] [10]

CB Configuration:



In common base configuration circuit is shown in figure. Here base is grounded and it is used as the common terminal for both input and output. It is also called as grounded base configuration. Emitter is used as a input terminal where as collector is the output terminal.

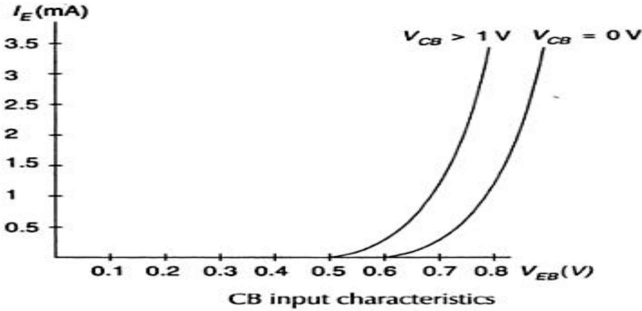
Input Characteristics

It is defined as the characteristic curve drawn between input voltage to input current whereas output voltage is constant.

To determine input characteristics, the collector base voltage V_{CB} is kept constant at zero and emitter current I_E is increased from zero by increasing V_{EB}.

This is repeated for higher fixed values of V_{CB}.

A curve is drawn between emitter current and emitter base voltage at constant collector base voltage is shown in figure.

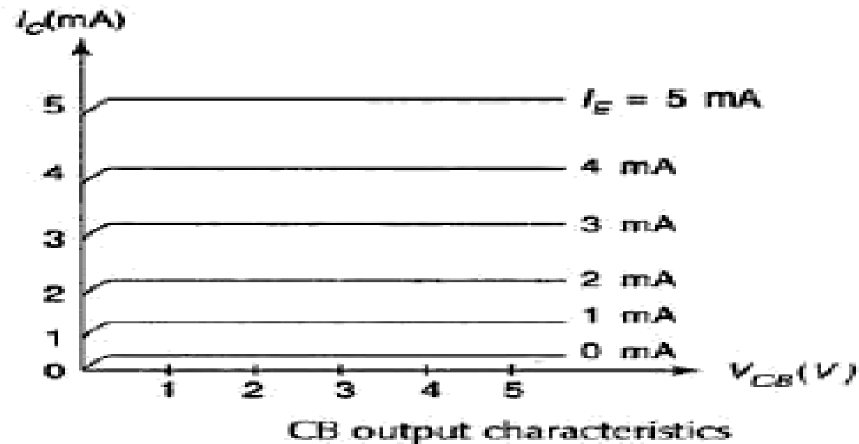


CB input characteristics

When V_{CB} is zero EB junction is forward biased. So it behaves as a diode so that emitter current increases rapidly.

Output Characteristics

It is defined as the characteristic curve drawn between output voltage to output current whereas input current is constant.



CB output characteristics

To determine output characteristics, the emitter current I_E is kept constant at zero and collector current Ic is increased from zero by increasing V_{CB}.

This is repeated for higher fixed values of I_E.

From the characteristic it is seen that for a constant value of I_E, Ic is independent of V_{CB} and the curves are parallel to the axis of V_{CB}.

As the emitter base junction is forward biased the majority carriers that is electrons from the emitter region are injected into the base region.

In CB configuration a variation of the base-collector voltage results in a variation of the quasi-neutral width in the base. The gradient of the minority-carrier density in the base therefore changes, yielding an increased collector current as the collector-base current is increased. This effect is referred to as the Early effect.

Transistor parameters in CB configuration

The slope of CB characteristics will give the following four transistor parameters. It is known as base hybrid parameters.

I. Input impedance (h_{ib}): It is defined as the ratio of change in input voltage (emitter voltage) to change in input current (emitter current) with the output voltage (collector voltage) is kept constant.

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}, V_{CB}\,Constant$$

This ranges from 20ohms to 50ohms.

II. Output admittance (h_{ob}): It is defined as the ratio of change in output current (collector current) to change in output voltage (collector voltage) with the input current (emitter current) is kept constant.

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}, I_E\,Constant$$

This ranges from 0.9 to 1.0.

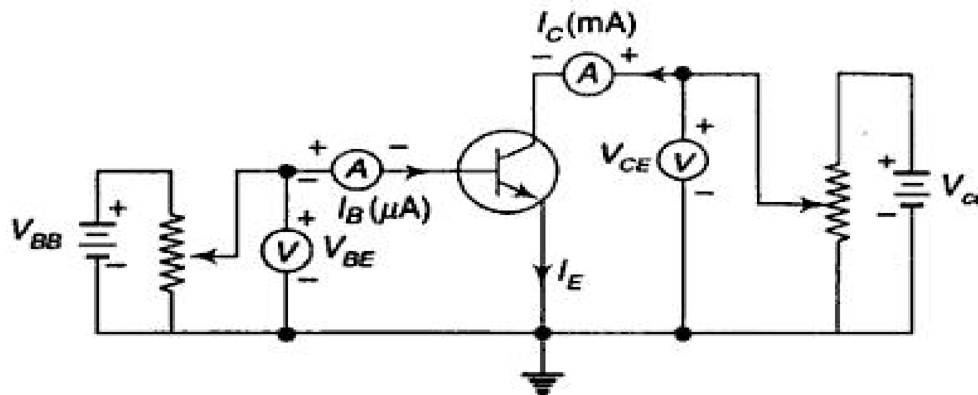
IV. Reverse voltage gain (h_{rb}): It is defined as the ratio of change in input voltage (emitter voltage) to change in output voltage (collector voltage) with the input current (emitter current) is kept constant.

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}, I_E\, Constant$$

This ranges from 10^{-5} to 10^{-4}.

3. Draw the circuit diagram of a NPN transistor CE configuration and the input and output characteristics. Also define its operating regions. [CO2 – L2 - May/June 2015] [12]

CE Configuration:



In common emitter configuration circuit is shown in figure. Here emitter is grounded and it is used as the common terminal for both input and output. It is also called as grounded emitter configuration. Base is used as a input terminal whereas collector is the output terminal.

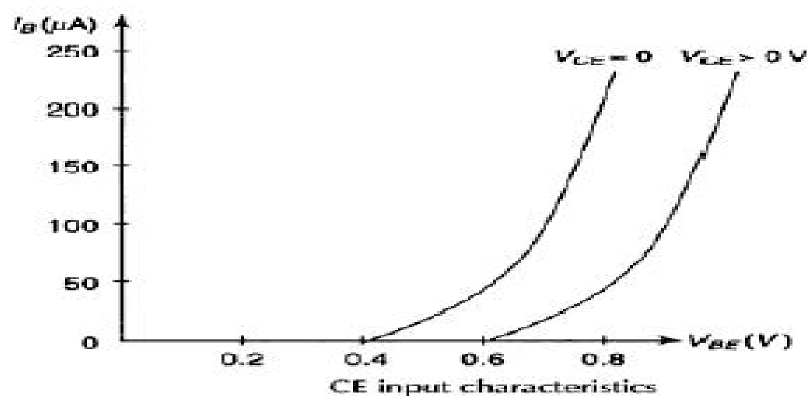
Input Characteristics

It is defined as the characteristic curve drawn between input voltage to input current whereas output voltage is constant.

To determine input characteristics, the collector base voltage V_{CB} is kept constant at zero and base current I_B is increased from zero by increasing V_{BE}.

This is repeated for higher fixed values of V_{CE}.

A curve is drawn between base current and base emitter voltage at constant collector base voltage is shown in figure.



CE input characteristics

.Here the base width decreases. So curve moves right as V_{CE} increases.

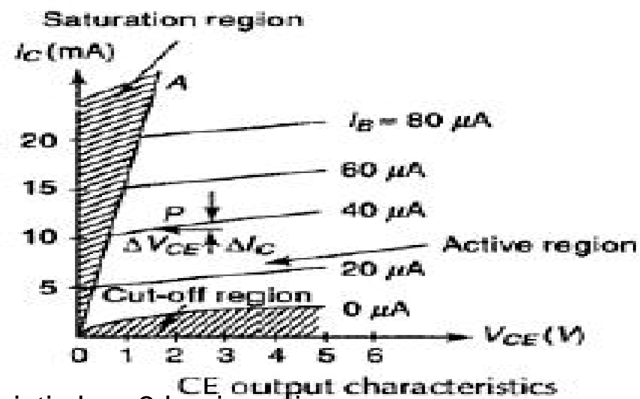
Output Characteristics

It is defined as the characteristic curve drawn between output voltage to output current whereas input current is constant.

To determine output characteristics, the base current I_B is kept constant at zero and collector current Ic is increased from zero by increasing V_{CE}.

This is repeated for higher fixed values of I_B..

From the characteristic it is seen that for a constant value of I_B, Ic is independent of V_{CB} and the curves are parallel to the axis of V_{CE}.



CE output characteristics

The output characteristic has 3 basic regions:

- Active region –defined by the biasing arrangements
- Cutoff region – region where the collector current is 0A
- Saturation region- region of the characteristics to the left of VCB = 0V

Transistor parameters in CE configuration

The slope of CE characteristics will give the following four transistor parameters. It is known as emitter hybrid parameters.

I. Input impedance (h_{ie}): It is defined as the ratio of change in input voltage (base voltage) to change in input current (base current) with the output voltage (collector voltage) is kept constant.

$$h_{ie} = \frac{\Delta V_{EB}}{\Delta I_B}, V_{CE}\, Constant$$

This ranges from 500ohms to 2000ohms.

II. Output admittance (h_{oe}): It is defined as the ratio of change in output current (collector current) to change in output voltage (collector voltage) with the input current (base current) is kept constant.

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}, I_B\, Constant$$

This ranges from 0.1 to 10µ mhos.

III. Forward current gain (h_{fe}): It is defined as the ratio of change in output current (collector current) to change in input current (base current) with the output voltage (collector voltage) is kept constant.

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}, V_{CE}\, Constant$$

This ranges from 20 to 200.

IV. Reverse voltage gain (h_{re}): It is defined as the ratio of change in input voltage (base voltage) to change in output voltage (collector voltage) with the input current (base current) is kept constant.

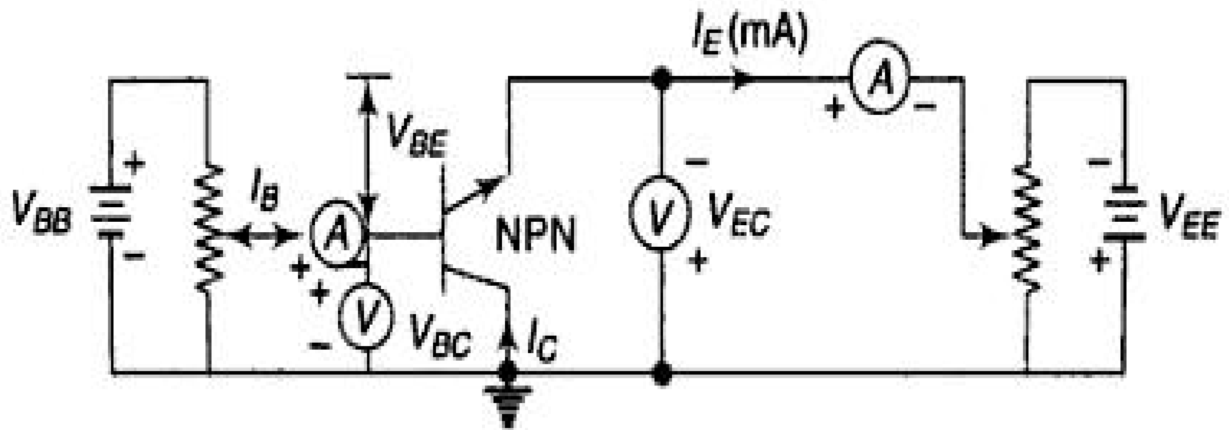
$$h_{re} = \frac{\Delta V_{EB}}{\Delta V_{CE}}, I_B\, Constant$$

This ranges from 10^{-5} to 10^{-4}.

4. Explain the input and output characteristics of a transistor in CC configuration.

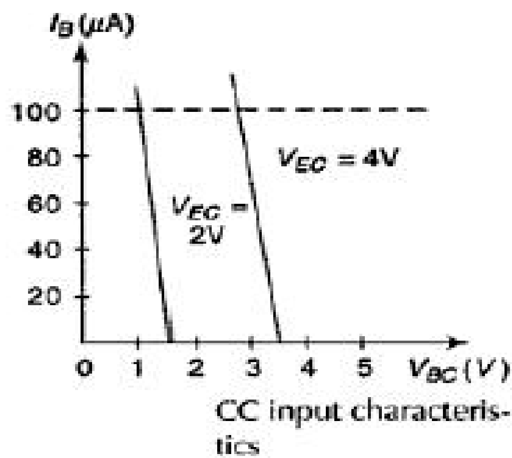
[CO2 – L2 - May/June 2013] [10]

CC Configuration:



In common collector configuration circuit is shown in figure. Here collector is grounded and it is used as the common terminal for both input and output. It is also called as grounded collector configuration. Base is used as a input terminal whereas emitter is the output terminal.

Input Characteristics



CC input characteristics

It is defined as the characteristic curve drawn between input voltage to input current whereas output voltage is constant. To determine input characteristics, the emitter base voltage V_{EB} is kept constant at zero and base current I_B is increased from zero by

This is repeated for higher fixed values of V_{CE}.

A curve is drawn between base current and base emitter voltage at constant collector base voltage is shown in above figure.

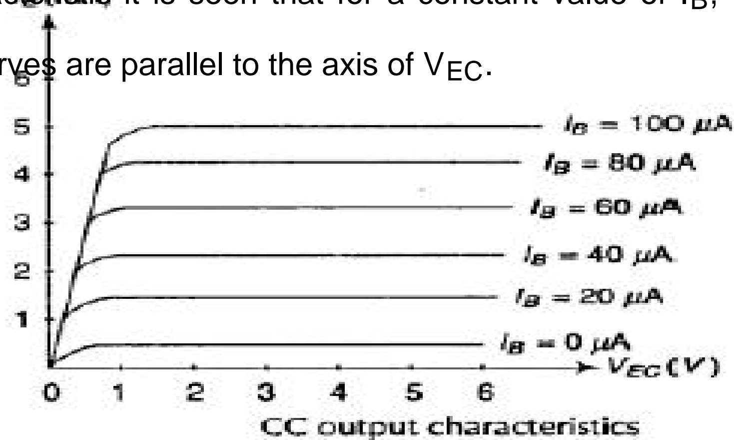
Output Characteristics

It is defined as the characteristic curve drawn between output voltage to output current whereas input current is constant.

To determine output characteristics, the base current I_B is kept constant at zero and emitter current I_E is increased from zero by increasing V_{EC}.

This is repeated for higher fixed values of I_B.

From the characteristic it is seen that for a constant value of I_B, I_E is independent of V_{EB} and the curves are parallel to the axis of V_{EC}.



CC output characteristics

Transistor parameters in CC configuration

The slope of CC characteristics will give the following four transistor parameters. It is known as base hybrid parameters.

I. Input impedance (h_{ic}): It is defined as the ratio of change in input voltage (base voltage) to change in input current (base current) with the output voltage (emitter voltage) is kept constant.

$$h_{ie} = \frac{\Delta V_{BC}}{\Delta I_B}, V_{CE}\, Constant$$

II. Output admittance (h_{oc}): It is defined as the ratio of change in output current (emitter current) to change in output voltage (emitter voltage) with the input current (base current) is kept constant.

$$h_{oe} = \frac{\Delta I_E}{\Delta V_{EC}}, I_B\, Constant$$

III Forward current gain (h_{fc}): It is defined as the ratio of change in output current (emitter current) to change in input current (base current) with the output voltage (emitter voltage) is kept constant.

$$h_{fc} = \frac{\Delta I_E}{\Delta I_B}, V_{CE}\, Constant$$

IV. Reverse voltage gain (h_{rc}): It is defined as the ratio of change in input voltage (base voltage) to change in output voltage (emitter voltage) with the input current (base current) is kept constant.

$$h_{rc} = \frac{\Delta V_{BC}}{\Delta V_{EC}}, I_B\, Constant$$

5. Give the comparison of CE, CB, CC configuration. [CO2 – H1 - May/June 2013] [6]

A comparison of CB, CE and CC Configurations

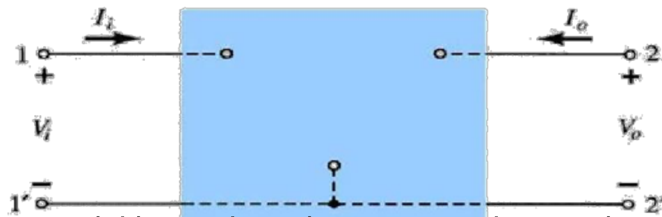
Property	***CB***	***CE***	**CC**
Input resistance	Low (about 100 O)	Moderate (about 750 Q)	High (about 750 kii)
Output resistance	High (about 450 kf2)	Moderate (about 45 ***kCl)***	Low (about 25 O)
Current gain	1	High	High
Voltage gain	About 150	About 500	Less than 1
Phase shift between input & output voltages	0 or 360°	180°	0 or 360°
Applications	for high frequency circuits	for audio frequency circuits	for impedance matching

6. Draw and explain the h-parameter Model for Bipolar Junction Transistor [CO2 – L2 - May/June 2015] [8]

H-Parameter BJT Model:

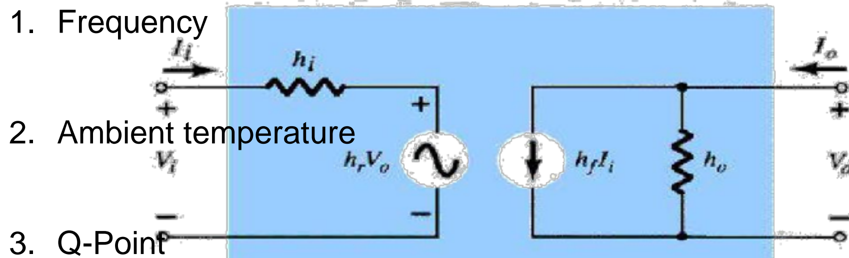
The h-parameter model is typically suited to transistor circuit modeling. It is important because:

1. its values are used on specification sheets
2. it is one model that may be used to analyze circuit behavior
3. it may be used to form the basis of a more accurate transistor model



Hybrid Equivalent Model

The h parameter model has values that are complex numbers that vary as a function of:



Hybrid Equivalent Circuit

1. Frequency
2. Ambient temperature
3. Q-Point

The revised two port network for the h parameter model is shown on the right. At low and mid-band frequencies, the h parameter values are real values. Other models exist because this model is not suited for circuit analysis at high frequencies

The h-parameter model is defined by:

$$V_1 = h_{11}I_1 + h_{12}V_2 \text{(KVL)}$$

$$I_2 = h_{21}I_1 + h_{22}V_2 \text{(KCL)}$$

The h-parameter model for the common emitter circuit is on the fig. On spec sheet:

$$h_{11} = h_{ix}$$

$$h_{12} = h_{rx}$$

$$h_{21} = h_{fx}$$

$$h_{22} = h_{ox}$$

. Explain briefly about the Gummel Poon model [CO2 – L2 - Nov/Dec 2015] [10]

- **Gummel-Poon Model:**

The Gummel-Poon model of the BIT considers more physics of the transistor that the Ebers-Moll model. This model can he used if, for example, there is a non-uniform doping concentration in the base.

The electron current density in the base of m npn transistor can be written as

An electric field will occur in the base if non uniform doping exists in the base. Electric field can be written as

$$E = \frac{KT}{e} \cdot \frac{l}{P(x)} \cdot \frac{dp(x)}{dx}$$

where p(x) is the majority carrier hole concentration in the base. Under low injection, the hole concentration is just the acceptor impurity concentration. With the doping profile shown in Figure. The electric field is negative (from the collector to the emitter). The direction of this electric field aids the flow of electrons across the base.

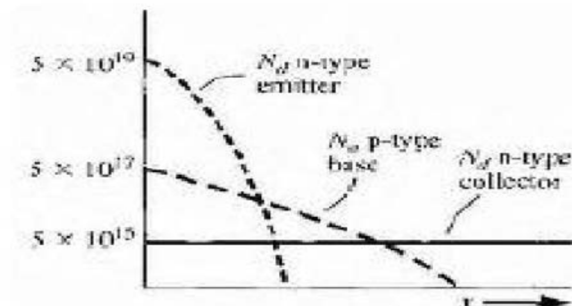
Substituting previous Equation we get

$$J_n = e\mu_n n(x). \frac{KT}{e} \cdot \frac{l}{P(x)} \cdot \frac{dp(x)}{dx} + eD_n \frac{dn(x)}{dx}$$

Using Einstein's relation, we can write Equation in the form

$$J_n = \frac{eD_n}{P(x)} \left[n(x) \frac{dP(x)}{dx} + P(x) \frac{dn(x)}{dx} \right] - \frac{eD_n}{P(x)} \frac{dP(n)}{dx}$$

$$J_n = e\mu_n n(x)\mathrm{E} + eD_n \frac{dn(x)}{dx}$$



Impurity concentration profiles of a double-diffused npn bipolar transistor.

It is written in the form of

$$\frac{J_n P(x)}{eD_n} = \frac{d(Pn)}{dx}$$

Integrating this eqn through the base

$$\frac{J_n}{eD_n}\int_0^{x\ \ B} P(x)dx - \int_0^{x_B} \frac{dP(x)}{dx}dx - P(x_B)n(x_B) - P(0)n(0)$$

The integral in the denominator is the total majority carrier charge in the base and is known as the base Gummel number; defined as Q_B.

The hole current density in the emitter of an NPN transistor can be expressed as,

$$J_P = \frac{-eD_p {n_i}^2 \exp\left(\frac{V_{BE}}{Vt}\right)}{\int_0^{xB} n(x)^2\, dx^2}$$

With the doping profile shown in Figure. The electric field is negative (from the collector to the emitter). The direction of this electric field aids the flow of electrons across the base.

The integral in the denominator is the total majority carrier charge in the emitter and is known as the emitter Gummel number, defined as Q_E.

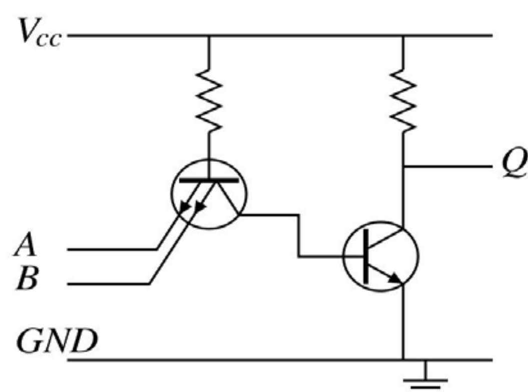
The Gummel-Poon model can also take into account non ideal effects, such as the Early effect and high-level injection.

If the B-E voltage becomes too large. low injection no longer applies, which leads to high-level injection. In this case, the total hole concentration in the base increases because of the increased excess hole concentration. This means that the base Gummel number will increase.

The Gummel-Poon model can then he used to describe the basic operation of the transistor as well as to describe non ideal effects.

8. How multi emitter transistor is working? Explain it with neat diagram. [CO2 – L2 - May/June 2015] [12

Multi Emitter Transistor (Transistor Transistor Logic):



TTL inputs are the emitters of a multiple-emitter transistor. This IC structure is functionally equivalent to multiple transistors where the bases and collectors are tied together. The output is buffered by a common emitter amplifier.

Inputs both logical ones. When all the inputs are held at high voltage, the base–emitter junctions of the multiple-emitter transistor are reverse-biased. Unlike DTL, a small ―collector‖ current (approximately 10µA) is drawn by each of the inputs. This is because the transistor is in reverse-active mode.

An approximately constant current flows from the positive rail, through the resistor and into the base of the multiple emitter transistor. This current passes through the base-emitter junction of the output transistor, allowing it to conduct and pulling the output voltage low (logical zero).

An input logical zero. Note that the base-collector junction of the multiple-emitter transistor and the base-emitter junction of the output transistor are in series between the bottom of the resistor and ground. If one input voltage becomes zero, the corresponding base-emitter junction of the multiple-emitter transistor is in parallel with these two junctions. A phenomenon called current steering means that when two voltage-stable elements with different threshold voltages are connected in parallel, the current flows through the path with the smaller threshold voltage. As a result, no current flows through the base of the output transistor, causing it to stop conducting and the output voltage becomes high (logical one). During the transition the input transistor is briefly in its active region; so it draws a large current away from the base of the output transistor and thus quickly discharges its base. This is a critical advantage of TTL over DTL that speeds up the transition over a diode input structure.

The main disadvantage of TTL with a simple output stage is the relatively high output resistance at output logical "1" that is completely determined by the output collector resistor. It limits the number of inputs that can be connected (the fanout). Some

advantage of the simple output stage is the high voltage level (up to V_{CC}) of the output logical "1" when the output is not loaded.

9. Explain details about the Ebers Moll model. [CO2 – L2 - May/June 2013] [12]

Ebers-Moll Model:

The Ebers-Moll model, or equivalent circuit, is one of the classic models of the bipolar transistor. This particular model is based on the interacting diode junctions and applicable in any of the transistor operating modes. Figure shows the current directions and voltage polarities used in the Ebers Moll model. The currents are defined as all entering the terminals so that

$$I_E + I_B + I_C = 0$$

The direction of the emitter current is opposite to what we have considered up to point, but as long as we are consistent in the analysis, the defined direction does not matter. The collector current can be written in general as

$$I_C = \alpha_F I_F - I_R$$

where α_F is the common base current rain in the forward-active mode. In this mode.

$$I_C = \alpha_F I_F + I_{CS}$$

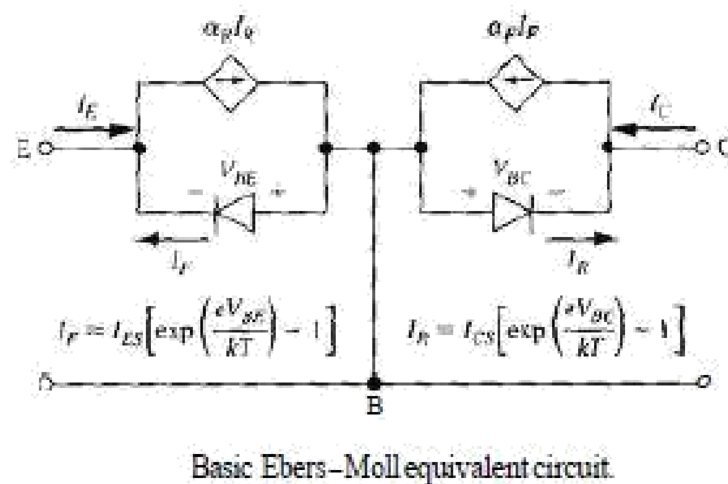
where the current I_{CS} is the reverse-bias B-C junction current. The current is given by

$$I_F = I_{ES}\left[exp^{\left(\frac{eV_E}{KT}\right)} - 1\right]$$

If the B-C junction becomes forward biased, such as in saturation, then we can write the current I_R as

$$I_R = I_{CS}\left[exp^{\left(\frac{eV_{BC}}{KT}\right)} - 1\right]$$

Using above equations collector current written as



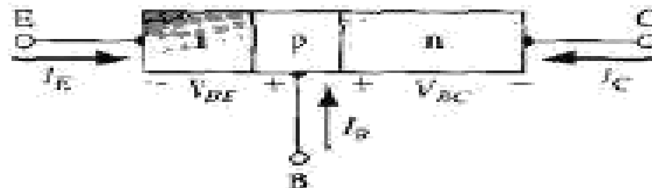
Basic Ebers–Moll equivalent circuit.

$$I_E = \alpha_R I_R - I_F$$

$$I_E = \alpha_R I_{CS}\left[\exp\left(\frac{eV_{BC}}{KT}\right) - 1\right] - I_{ES}[\exp\left(\frac{eV_{BE}}{KT}\right) - 1]$$

The current IEs is the reverse-bias B-E junction current and u~ is the common base current gain for the inverse-active mode. The current sources in the equivalent circuit represent current components that depend on voltages across other junctions. The Ebers-Moll model has four parameters: α_F, α_R, I_{ES} and Ics. However, only three parameters are independent. The reciprocity relationship states that

Normally in electronic circuit applications, the collector-emitter voltage at saturation is of interest. We can define the C-E saturation voltage as
Combining the previous some eqn we get



Current direction and voltage polarity definitions for the Ebers–Moll model.

$$I_E = \alpha_R I_{CS}\left[\exp\left(\frac{eV_{BC}}{KT}\right) - 1\right] - I_{ES}[\exp\left(\frac{eV_{BE}}{KT}\right) - 1]$$

If we solve for the value of and sub in previous one and simplifying we get

$$I_E = \alpha_R I_{CS}\left[\exp\left(\frac{eV_{BC}}{KT}\right) - 1\right] - I_{ES}[\exp\left(\frac{eV_{BE}}{KT}\right) - 1]$$

The ratio of Ics to I_Es can be written in terms of α_F and α_R and we finally get

$$V_{BE} = V_T l_n[I_C(1-\alpha_R) + I_B + I_{ES}(1-\alpha_F C_R)/I_{ES}(1-\alpha_F\alpha_R]$$

$$V_{CE}(\text{sat}) = V_T l_n[\frac{I_C(1-\alpha_R) + I_B}{\alpha_F I_B - (1-\alpha_F)I_C}.\frac{\alpha_F}{\alpha_R}$$

Unit - III

Field Effect Transistors

Part - A

1. Why it is called field effect transistor? [CO3 – L2 - May/June 2013]

The drain current I_D of the transistor is controlled by the electric field that extends into the channel due to reverse biased voltage applied to the gate, hence this device has been given the name Field Effect Transistor.

2. Why FET is called voltage controlled device. [CO3 – L2 - May/June 2014]

FET the value of the current depends upon the value of the voltage applied at the ate and drain. So it is *known as voltage controlled device*.

3. Define the term threshold voltage. [CO3 – L2 - Nov/Dec 2013]

The **threshold voltage**, commonly abbreviated as $\mathbf{V_{th}}$, of a field-effect transistor (FET) is the value of the gate–source voltage when the conducting channel just begins to connect the source and drain contacts of the transistor, allowing significant current.

The threshold voltage of a junction field-effect transistor is often called **pinch-off voltage** instead, which is somewhat confusing since "pinch off" for an insulated-gate field-effect transistor is used to refer to the channel pinching that leads to current saturation behavior under high source–drain bias, even though the current is never off. The term "threshold voltage" is unambiguous and refers to the same concept in any field-effect transistor.

4. What is channel length modulation? [CO3 – L2 - May/June 2014]

One of several short-channel effects in MOSFET scaling, **channel length modulation** (**CLM**) is a shortening of the length of the inverted channel region with increase in drain bias for large drain biases.

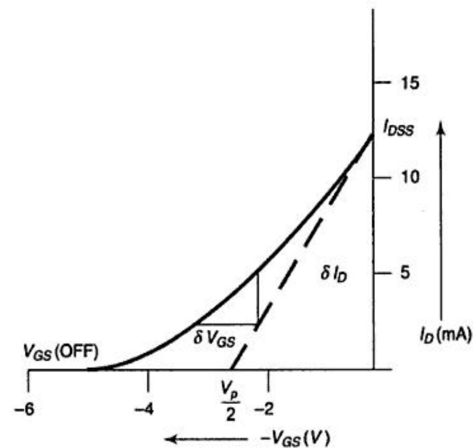
As the drain voltage increases, its control over the current extends further toward the source, so the un inverted region expands toward the source, shortening the length of the channel region, the effect called *channel-length modulation*.

5. Compare JFET with BJT. [CO3 – L2 - May/June 2015]

- FET operation depends only on the flow of majority carriers-holes for P-channcl FETs and electrons for N-channel FETs. Therefore, they arc called Unipolar devices. Bipolar transistor (BJT) operation depends on both minority and majority current carriers.
- As FET has no junctions and the conduction is through an N-type or P-type semiconductor material. FET is less noisy than BJT.
- As the input circuit of FET is reverse biased, FET exhibits a much higher input impedance (in the order of 100 M *)* and lower output impedance and there will be a high degree of isolation between input and output. So. FET can act as an excellent buffer amplifier but the BJT has low input impedance because its input circuit is forward biased.
- FET is a voltage controlled device, i.e. voltage at the input terminal controls the output current, whereas BJT is a current controlled device, i.e. the input current controls the output current.

- FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.

6. Draw the transfer characteristics curve for JFET. [CO3 – L2 - May/June 2015]



7. Differentiate between N and P channel FETs [CO3 – L2 - Nov/Dec 2014]

1. In an N channel JFET the current carriers are electrons, whereas the current carriers are holes in a P channel JFET.

2. Mobility of electrons is large in N channel JFET; Mobility of holes is poor in P channel JFET.

3. The input noise is less in N channel JFET than that of P channel JFET.

4. The transconductance is larger in N channel JFET than that of P channel JFET.

8. Write some applications for JFET. [CO3 – L3 - May/June 2013]

1. FET is used as a buffer in measuring instruments, receivers since it has high input impedance and low output impedance.
2. FETs arc used in RF amplifiers in FM tuners and communication equipment for the low noise level.
3. Since the input capacitance is low. FETs are used in cascade amplifiers in measuring and test equipments.
4. Since the device is voltage controlled, it is used as a voltage variable resistor in operational amplifiers and tone controls.
5. FETs are used in mixer circuits in FM and TV receivers, and communication equipment because inter modulation distortion is low.

9. Compare MOSFET with JFET. [CO3 – L2 - May/June 2015]

- In enhancement and depletion types of MOSFET. the transverse lectric field induced across an insulating layer deposited on the semiconductor material controls the conductivity of the channel. In the JFET the transverse electric field across the reverse biased PN junction controls the conductivity of the channel.
- The gate leakage current in a MOSFET is of the order of 10^{12} A. Hence the input resistance of a MOSFET is very high in the order of $I0^{10}$ to $I0^{W}$ ***iI.*** The gate leakage current of a JFET is of the order of $I0"^{9}$ A and its input resistance is of the order of 10* ft.
- The output characteristic* of the JFET are flatter than those of the MOSFET and hence, the drain resistance of a JFET (0.1 to I) is much higher than that of a MOSFET (I to 50).
- JFETs arc operated only in the depletion mode. The depletion type MOSFET may be operated in both depletion and enhancement mode.

- Comparing to JFET. MOSFETs are easier to fabricate.

10. Compare N channel MOSFET with P channel MOSFET. [CO3 – L2 - May/June 2014]

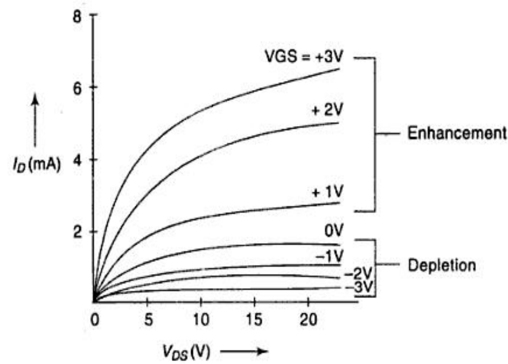
- The P-channel enhancement MOSFET is very popular because it is much easier and cheaper to produce than the N-channel device.
- The hole mobility is nearly 2.5 times lower than the electron mobility. Thus, a P-channel MOSFET occupies a larger area than an N-channel MOSFET having the same I_n rating.
- The drain resistance of P-channcl MOSFET is three times higher than that for an identical N-channel MOSFET.
- The N-channel MOSFET has the higher packing density which makes it faster in switching applications due to the smaller junction areas and lower inherent capacitances.
- The N-channel MOSFET is smaller for the same complexity than P-channcl device.

11. Differentiate between current voltage relationships of the N channel and P channel MOSFET [CO3 – L2 – Nov/Dec2013]

N-Oumnel MOSFET	P-Channel MOSFET
Saturation region {$V_{I)S} > V_{D5}$(sat))	Saturation region [$V_{sn} > Vy$, (sat))

Non saturation region (V^j < V^saO) /z>=^I2(V_{cs}-V_M.)V_M-^s]	Non saturation region (V^ < V^sat)) t_D = (Vs_C+V_{TP})V_{SD}-Vl_s]
Transition point V,„(sa>I = I',, - V„	Transition point IfafM-Ib<» V„
Enhancement mode V„>0	Enhancement mode W, < 0
Depletion mode Vt» < 0	Depiction mode V_7, > (»

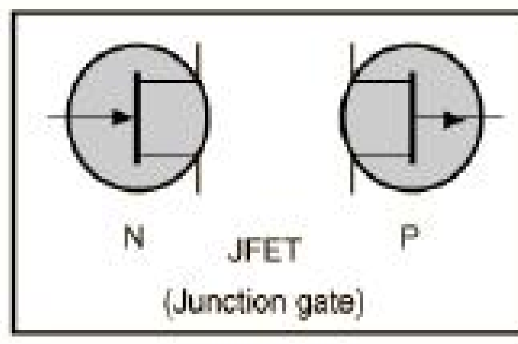
12. Draw the V-I characteristics curve of MOSFET. [CO3 – L2 - May/June 2013]



PART B

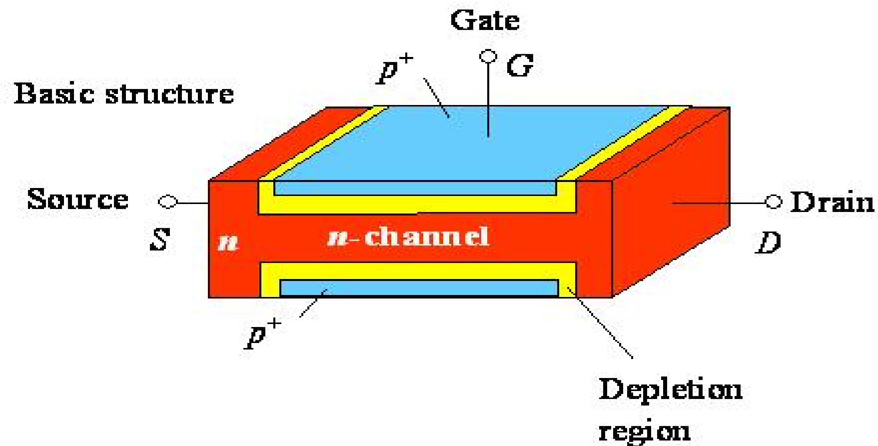
1. Explain the operation of JFET and derive the drain and transfer characteristics. [CO3 – L2 - May/June 2014] [16]

Junction FETs (JFETs)



JFETs consists of a piece of high-resistivity semiconductor material (usually Si) which constitutes a channel for the majority carrier flow.Conducting semiconductor channel between two ohmic contacts – source & drain.JFET is a high-input resistance device, while the BJT is comparatively low.

If the channel is doped with a donor impurity, n-type material is formed and the channel current will consist of electrons.



If the channel is doped with an acceptor impurity, p-type material will be formed and the channel current will consist of holes.

N-channel devices have greater conductivity than p-channel types, since electrons have higher mobility than do holes; thus n-channel JFETs are approximately twice as efficient conductors compared to their p-channel counterparts.

The magnitude of this current is controlled by a voltage applied to a gate, which is a reverse-biased.

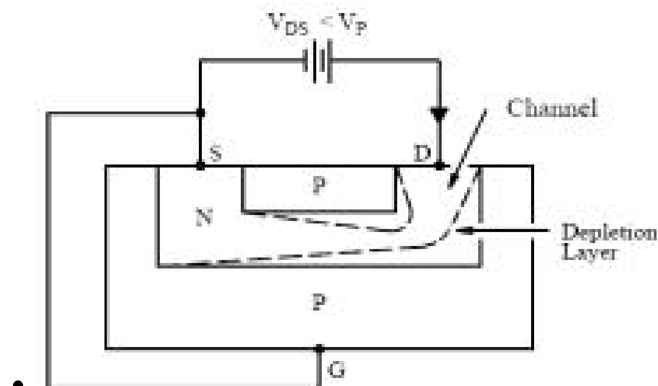
The fundamental difference between JFET and BJT devices: when the JFET junction is reverse-biased the gate current is practically zero, whereas the base current of the BJT is always some value greater than zero.

Basic structure of JFETs

- In addition to the channel, a JFET contains two ohmic contacts: the source and the drain.
- The JFET will conduct current equally well in either direction and the source and drain leads are usually interchangeable. N-channel JFET
- This transistor is made by forming a channel of N-type material in a P-type substrate.
- Three wires are then connected to the device.
- One at each end of the channel.
- One connected to the substrate.

In a sense, the device is a bit like a PN-junction diode, except that there are two wires connected to the N-type sideThe gate is connected to the source.

- Since the pn junction is reverse-biased, little current will flow in the gate connection.



- The potential gradient established will form a depletion layer, where almost all the electrons present in the n-type channel will be swept away. The most depleted portion is in the high field between the G and the D, and the least-depleted area is between the G

and the S.

- Because the flow of current along the channel from the (+ve) drain to the (-ve) source is really a flow of free electrons from S to D in the n-type Si, the magnitude of this current will fall as more Si becomes depleted of free electrons.
- There is a limit to the drain current (ID) which increased VDS can drive through the channel.
- This limiting current is known as IDSS (*Drain-to-Source current with the gate shorted to the source*).
- The output characteristics of an n-channel JFET with the gate short-circuited to the source.
- The initial rise in ID is related to the buildup of the depletion layer as VDS increases.
- The curve approaches the level of the limiting current IDSS when ID begins to be pinched off.
- The physical meaning of this term leads to one definition of pinch-off voltage, VP , which is the value of VDS at which the maximum IDSS flows.
- With a steady gate-source voltage of 1 V there is always 1 V across the wall of the channel at the source end.
- A drain-source voltage of 1 V means that there will be 2 V across the wall at the drain end.

(The drain is ‗up‘ 1V from the source potential and the gate is 1V ‗down‘, hence the total difference is 2V.)

• The higher voltage difference at the drain end means that the electron channel is squeezed down a bit more at this end.

• When the drain-source voltage is increased to 10V the voltage across the channel walls at the drain end increases to 11V, but remains just 1V at the source end.

• The field across the walls near the drain end is now a lot larger than at the source end.

• As a result the channel near the drain is squeezed down quite a lot.

• Increasing the source-drain voltage to 20V squeezes down this end of the channel still

more.As we increase this voltage we increase the electric field which drives electrons along the open part of the channel. However, also squeezes down the channel near the drain end. This reduction in the open channel width makes it harder for electrons to pass.

• As a result the drain-source current tends to remain constant when we increase the drain source voltage.

• Increasing V_{DS} increases the widths of depletion layers, which penetrate more into channel and hence result in more channel narrowing toward the drain.

• The resistance of the n-channel, R_{AB} therefore increases with V_{DS}.

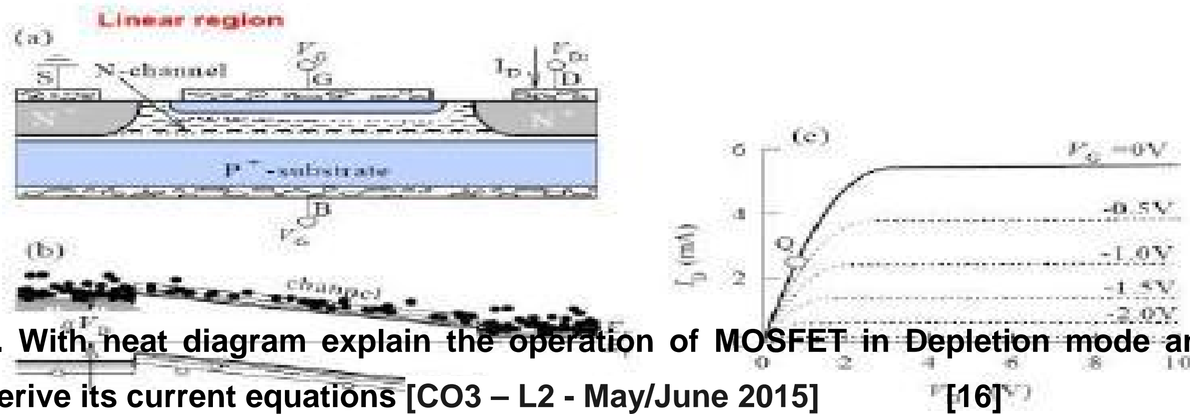
• The drain current: $I_{DS} = V_{DS}/R_{AB}$

• I_D versus V_{DS} exhibits a sub linear behavior, see figure for $V_{DS} < 5V$.

• The pinch-off voltage, V_P is the magnitude of reverse bias needed across the p_+n junction to make them just touch at the drain end.

• Since actual bias voltage across p_+n junction at drain end is V_{GD}, the pinch-off occur whenever: $V_{GD} = -V_P$.

JFET: I-V characteristics



2. With neat diagram explain the operation of MOSFET in Depletion mode and derive its current equations [CO3 – L2 - May/June 2015] [16]

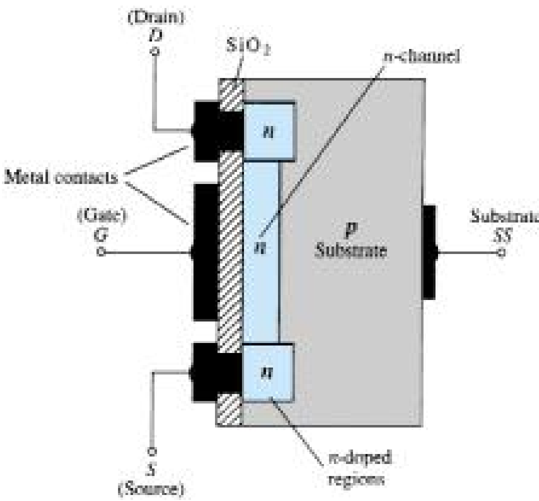
Depletion-Type MOSFET

MOSFETs are further broken down into depletion type and enhancement type. The terms depletion and enhancement define their basic mode of operation, while the label MOSFET stands for metal-oxide-semiconductor-field-effect transistor.

Basic Construction

The basic construction of the n-channel depletion-type MOSFET is provided in Fig. A

slab of p-type material is formed from a silicon base and is referred to as the substrate. It is the foundation upon which the device will be constructed. In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labeled SS, resulting in a four-terminal device, such as that appearing in Fig. 1



The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a particular type of insulator referred to as a dielectric that sets up opposing (as revealed by the prefix di-) electric fields within the dielectric when exposed to an externally applied field.

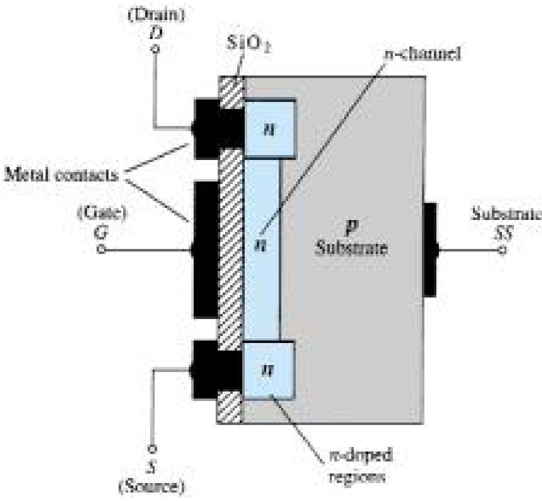


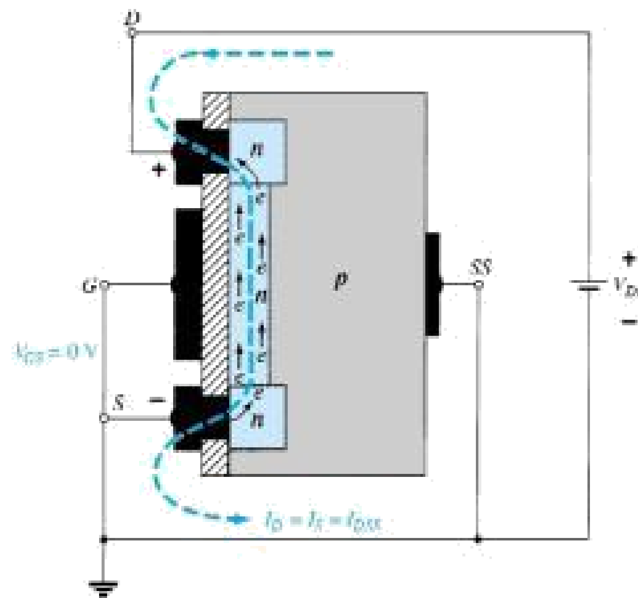
Fig 2. n – channel depletion type MOSFET with V_{GS} = 0 V

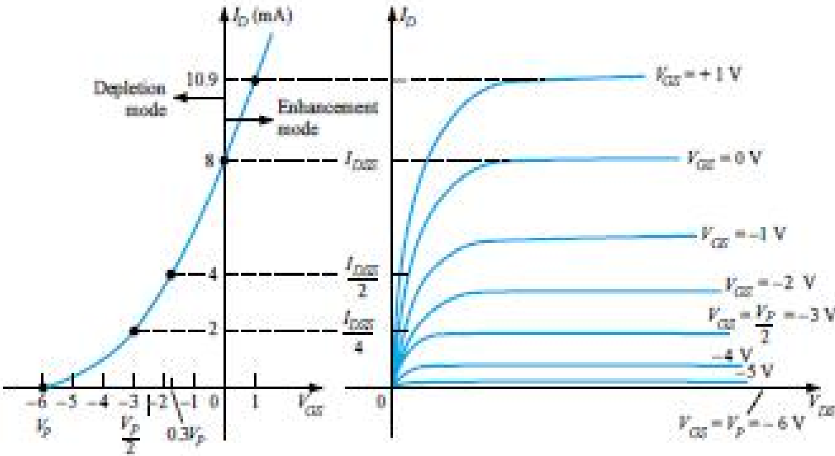
There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

It is the insulating layer of SiO2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

Basic Operation and Characteristics

In Fig. 2 the gate-to-source voltage is set to zero volts by the direct connection from one terminal to the other, and a voltage VDS is applied across the drain-to-source terminals. The result is an attraction for the positive potential at the drain by the free electrons of the n-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with V_{GS} = 0 V continues to be labeled IDSS, as shown in Fig. 3.Fig 2. n – channel depletion type MOSFET with V_{GS} = 0 V




I_D (mA)
I_D
10.9
Depletion mode
Enhancement mode
8
I_{DSS}
4
$\frac{I_{DSS}}{2}$
2
$\frac{I_{DSS}}{4}$
V_{GS} = +1 V
V_{GS} = 0 V
V_{GS} = −1 V
V_{GS} = −2 V
$V_{GS} = \frac{V_P}{2}$ = −3 V
−4 V
−5 V
$V_{GS} = V_P$ = − 6 V
V_{GS}
V_{DS}
V_P
$\frac{V_P}{2}$
$0.3V_P$

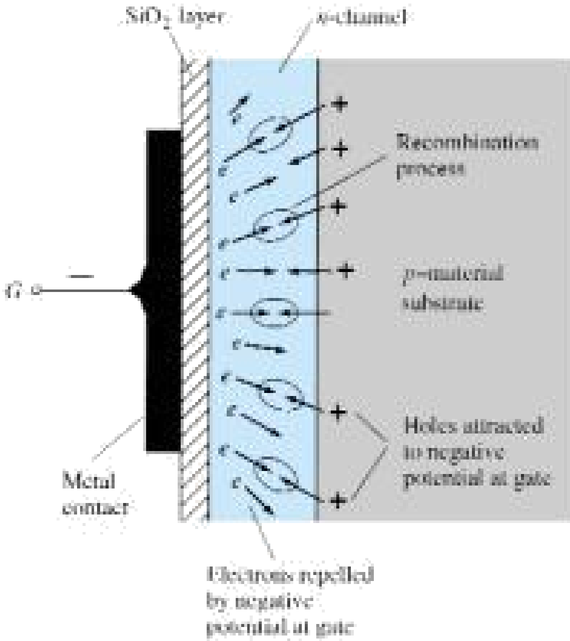

SiO_2 layer
n-channel
Recombination process
p-material substrate
Holes attracted to negative potential at gate
G
Metal contact
Electrons repelled by negative potential at gate

Fig.4 Reduction in free carriers in channel due to –ve potential

In Fig. 4, VGS has been set at a negative voltage such as -1 V. The negative potential at the gate will tend to pressure electrons toward the p-type substrate (like charges repel) and attract holes from the p-type substrate (opposite charges attract) as shown in Fig. 4. Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, the higher the rate of recombination.

For positive values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the p-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. 3 reveals that the drain current will increase at a rapid rate.

3. With neat diagram explain the operation of MOSFET in Enhancement mode and derive its current equations [CO3 –H1 - Nov/Dec 2013] [16]

Enhancement-Type MOSFET:

Basic Construction

The basic construction of the n-channel enhancement-type MOSFET is provided in Fig.1. A slab of p-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, while in other cases a fourth lead is made available for external control of its potential level.

The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material. In summary, therefore, the construction of an enhancement-type

MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

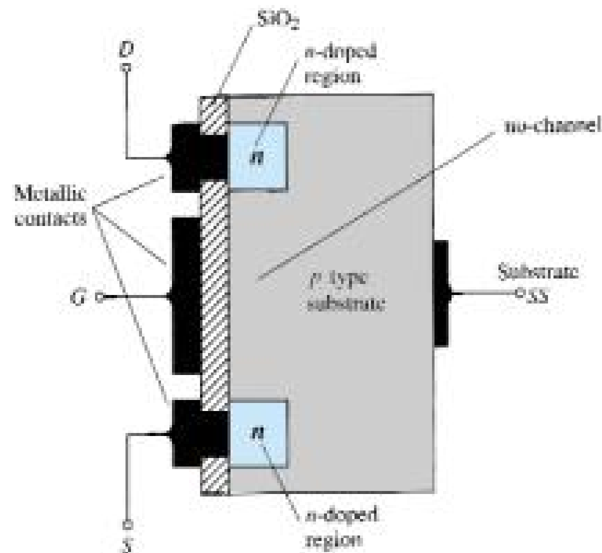
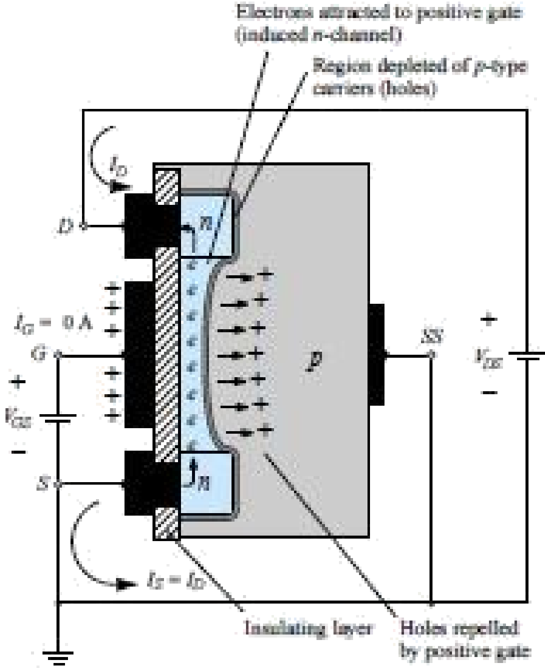


Fig 1. N channel enhancement type MOSFET

Basic Operation and Characteristics

If V_{GS} is set at 0 V and a voltage applied between the drain and source of the device of Fig. 1, the absence of an n-channel (with its generous number of free carriers) will result in a current of effectively zero amperes—quite different from the depletion- type MOSFET and JFET where I_D - I_{DSS}. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and source (due to the n-doped regions) if a path fails to exist between the two. With VDS some positive voltage, VGS at 0 V, and terminal SS directly connected to the source, there are in fact two reverse-biased p-n junctions between the n-doped regions and the p-substrate to oppose any significant flow between drain and source.



In Fig. 2 both VDS and VGS have been set at some positive voltage greater than 0 V, establishing the drain and gate at a positive potential with respect to the source. The positive potential at the gate will pressure the holes (since like charges repel) in the p-substrate along the edge of the SiO2 layer to leave the area and enter deeper regions of the p-substrate, as shown in the figure.

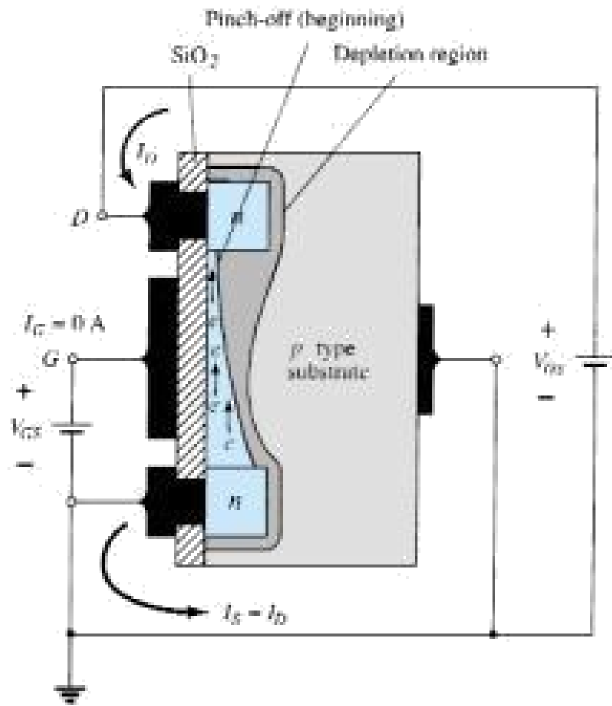


Fig 2. Channel formation

As *VGS* is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold *VGS* constant and increase the level of *VDS*, the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The leveling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 3. Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 3, we find that

$$V_{DG} = V_{DS} - V_{GS}$$

The drain characteristics of Fig. 5.34 reveal that for the device of Fig 3 with VGS = 8 V, saturation occurred at a level of VDS = 6 V. In fact, the saturation level for VDS is related to the level of applied VGS by

$$V_{DSsat} = V_{GS} - V_T$$

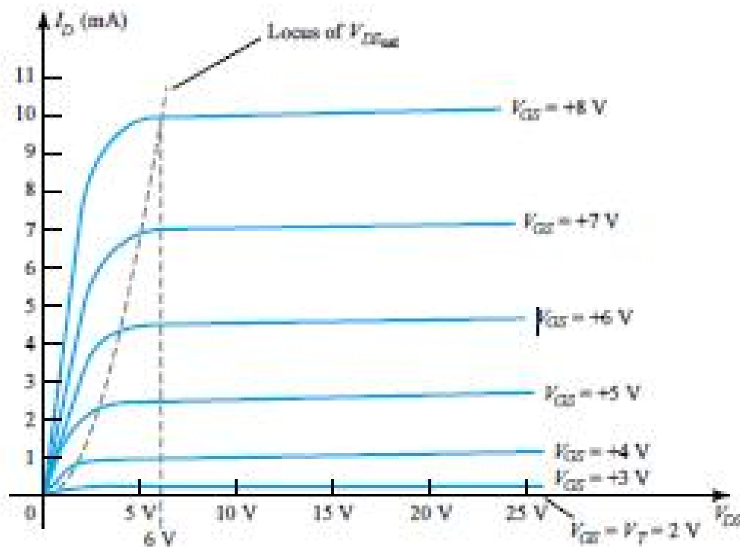


Fig 4. Drain characteristics

For levels of VGS > VT, the drain current is related to the applied gate-to-source voltage by the
following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2$$

Again, it is the squared term that results in the nonlinear (curved) relationship between ID and VGS. The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation where ID(on) and VGS(on) are the values for each at a particular point on the characteristics of the device.

4. Give some characteristics of MOSFET. [CO3 – L2 - Nov/Dec 2014] [8]

MOSFET I-V CHARACTERISTICS

1. H
ook up the circuit of Fig. 2. This circuit will be used in the following steps to investigate the i-v characteristics of the n-channel MOSFET. The chip used in this experiment is a CD4007, containing six MOSFETs. We will use only one of them, as shown in the pin assignment in Fig. 3. Figure 3 2.
2. Set vGS = 5 V Measure the drain current iDS, versus the drain-source voltage, vDS, from 0 to 5 V Make sure you take measurements at a sufficient number of vDS values since you will later need to plot iDS versus vDS. Include a point at vDS = 0.1 V for later use.
3. 3. Repeat the entire step 2 for vGS = 3 V and vDS = 1 V. 1 It should be noted that the only DC current in the device is the drain-to-source current iDS. The gate is internally separated by an insulator from the channel, so the gate current is practically zero.
4. 4. With vDS = 5 V, determine the value of vGS at which the current iDS becomes negligible; assume that for our purposes this means 5mA. This value of vGS is close to the so-called threshold voltage of the transistor, and it is positive for an "enhancement mode" MOSFET, which is what we are working with here.2
5. 5. Using the data you have collected in steps 2 and 3, plot a family of curves for the drain current, iDS, versus the drain-source voltage, vDS from 0 to 5 V, with vGS as a parameter. Use a single set of vDS - iDS axes for this plot. There should be one curve for each vGS value (1 V, 3 V, and 5 V) on this family of curves. Label each curve with the corresponding vGS value.
6.

   6. You should be able to observe on the above plot that, for each curve, the current tends to a constant (or, as we say, saturates) as

vDS is made large. What is, approximately, the saturation value of the current for each of the three vGS values.

5. Explain the operation of dual gate MOSFET [CO3 – L2 - Nov/Dec 2015] [8]

One form of MOSFET that is particularly popular in many RF applications is the dual gate MOSFET. The dual gate MOSFET is used in many RF and other applications where two control gates are required in series.

The dual gate MOSFET is essentially a form of MOSFET where two gates are fabricated along the length of the channel - one after the other. In this way, both gates affect the level of current flowing between the source and drain.

In effect, the dual gate MOSFET operation can be considered the same as two MOSFET devices in series. Both gates affect the overall MOSFET operation and hence the output. In effect, the dual gate MOSFET operation can be considered the same as two MOSFET devices in series. Both gates affect the overall MOSFET operation and hence the output.

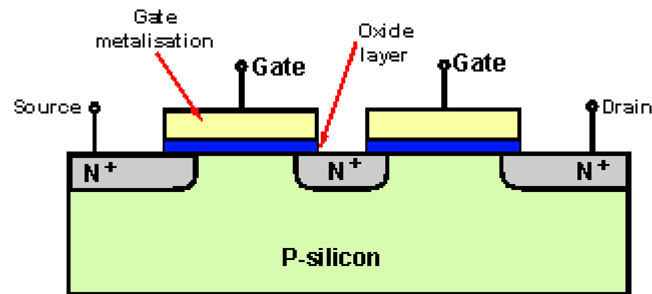
Dual gate MOSFET circuit symbol

The dual gate MOSFET can be used in a number of applications including RF mixers /multipliers, RF amplifiers, amplifiers with gain control and the like.

Dual gate MOSFET structure

The dual gate MOSFET has what may be referred to as a tetrode construction where the two grids control the current through the channel.

The different gates control different sections of the channel which are in series with each other.



Dual gate MOSFET structure

Dual gate MOSFET amplifier

Dual gate MOSFETs are able to operate with improved performance as amplifiers over single gated FETs. The dual gate MOSFET enables a cascode two stage amplifier to be constructed using a single device.

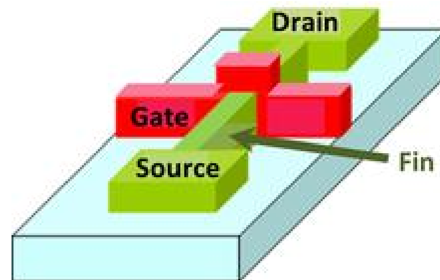
The cascade amplifier helps overcome the Miller effect where capacitance is present between the input and output stages. Although the Miller effect can relate to any impedance between the input and output, normally the most critical is capacitance. This capacitance can lead to an increase in the level of input capacitance experienced and in high frequency (e.g. VHF & UHF) amplifiers it can also lead to instability.

The effect is overcome by using a cascade amplifier using a single dual gate FET. In this configuration, biasing the drain-side gate at constant potential reduces the gain loss caused by Miller effect. The effects of capacitive coupling between the input and output are virtually eliminated.

The method of implementation of the dual gate MOSFET amplifier can be seen in the diagram below.

In this circuit the lower or input FET section is in a self-biased, common-source configuration. The upper or output FET section is configured in a in a voltage-divider biased, common-gate configuration.

6. Explain the operation of FINFET [CO3 – L2 - May/June 2015] [8]



FINFET:

The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the body of the device. The thickness of the fin (measured in the direction from source to drain) determines the effective channel length of the device. In current usage the term FinFET has a less precise definition. Among microprocessor manufacturers, AMD, IBM, and Motorola describe their double-gate development efforts as FinFET] development whereas Intel avoids using the term to describe their closely related tri-gate architecture. In the technical literature, FinFET is used somewhat generically to describe any fin-based, multigate transistor architecture regardless of number of gates.

A 25-nm transistor operating on just 0.7 volt was demonstrated in December 2002 by Taiwan Semiconductor Manufacturing Company. The "Omega FinFET" design is named after the similarity between the Greek letter omega (Ω) and the shape in which the gate wraps around the source/drain structure. It has a gate delay of just 0.39 picosecond (ps) for the N-type transistor and 0.88 ps for the P-type. FinFET can also have two electrically independent gates, which gives circuit designers more flexibility to design with efficient, low-power gates. [12]

Unit - IV

Special Semiconductor Devices

Part - A

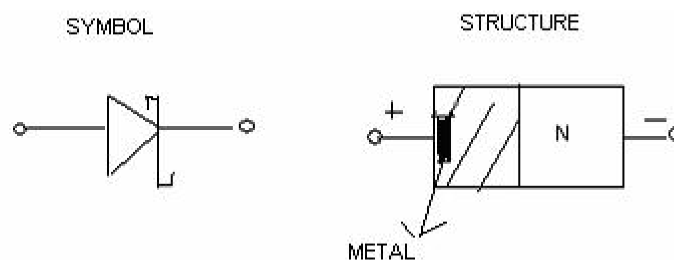
1. What is a metal semiconductor contact? [CO4 – L1 - Nov/Dec 2015]

A metal semiconductor contact is a contact between a metal and a semiconductor which according to the doping level and requirement may act as a rectifying diode or just a simple contact between a semiconductor device and the outside world.

2. Define contact potential in metal semiconductor contact. [CO4 – L2 - May/June 2015]

The difference of potential between the work function of metal and the work function of semiconductor in a metal semiconductor contact is termed as contact potential.

3. Give the symbol and structure of schottky diode. [CO4 – L1 - May/June 2014]



4. Give the applications of schottky diode. [CO4 – L1 - Nov/Dec 2013]

1. It can switch off faster than bipolar diodes

2. It is used to rectify very high frequency signals (>10 MHZ)
3. as a switching device in digital computers.

4. It is used in clipping and clamping circuits.
5. It is used in communication systems such as frequency mixers, modulators and detectors.

5. Compare between schottky diode and conventional diode. [CO4 – L2 - Nov/Dec 2014]

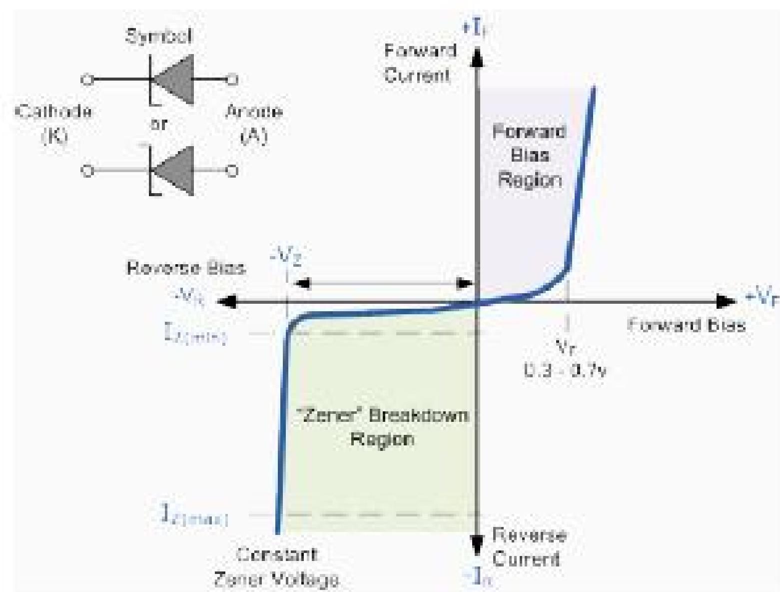
PN junction diode	Schottky diode
1. Here the contact is established between two semiconductors	1. Here the contact is established between the semiconductor and metal
2. current conduction is due to both majority and minority carriers	2. current conduction is only due to majority carriers
3. large reverse recovery time	3. Small reverse recovery time
4. barrier potential is high about 0.7 V	4. Barrier potential is low about 0.25 V
5. switching speed is less	5. switching speed is high
6. cannot operate at high frequency	6. can operate at very high frequency (> 300MHz)

6. Why zener diode is often preferred than PN diode. [CO4 – L2 - Nov/Dec 2013]

When the reverse voltage reaches breakdown voltage in normal PN junction diode the current through the junction and the power dissipated at the junction will high. Such an operation is destructive and the diode gets damaged.

Whereas diode can be designed with adequate power dissipation capabilities to operate in breakdown region. That diode is known as zener diode. It is heavily doped than ordinary diode.

7. Draw the V-I characteristics curve for zener diode. [CO4 – L1 - May/June 2013]



8. What is zener breakdown? [CO4 – L1 - Nov/Dec 2015]

Zener break down takes place when both sides of the junction are very heavily doped and Consequently the depletion layer is thin and consequently the depletion layer is tin. When a small value of reverse bias voltage is applied , a very strong electric field is set up across the thin depletion layer. This electric field is enough to break the covalent bonds. Now extremely large number of free charge carriers are produced which constitute the zener current. This process is known as zener break down.

9. What is avalanche break down? [CO4 – L1 - Nov/Dec 2013]

When bias is applied, thermally generated carriers which are already present in the diode acquire sufficient energy from the applied potential to produce new carriers by removing valence electron from their bonds. These newly generated additional carriers acquire more energy from the potential and they strike the lattice and create more number of free electrons and holes. This process goes on as long as bias is increased and the number of free carriers get multiplied. This process is termed as avalanche multiplication. Thus the break down which occur in the junction resulting in heavy flow of current is termed as avalanche break down.

10. What is tunneling phenomenon? [CO4 – L1 - Nov/Dec 2016]

The phenomenon of penetration of the charge carriers directly though the potential barrier instead of climbing over it is called as tunneling.

11. Give the application of tunnel diode. [CO4 – L1 - May/June 2015]

- As logic memory storage device
- As microwave oscillator
- In relaxation oscillator circuit

- As an amplifier
- As an ultra-high speed switch

12. Give the advantages and disadvantages of tunnel diode Advantages [CO4 – L1]

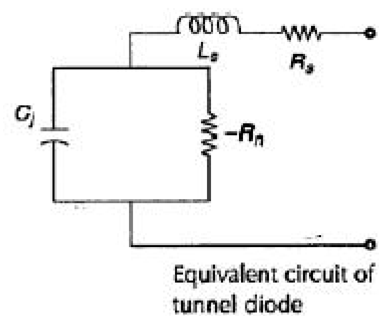
Advantages

- Low noise
- Ease of operation
- High speed
- Low power

Disadvantages

- Voltage range over which it can be operated is 1 V less.
- Being a two terminal device there is no isolation between the input and output circuit.

13. Draw equivalent circuit of tunnel diode [CO4 – L1]



Equivalent circuit of tunnel diode

• This is the equivalent circuit of tunnel diode when biased in negative resistance region.

• At higher frequencies the series R and L can be ignored.

• Hence equivalent circuit can be reduced to parallel combination of junction capacitance and negative resistance.

14. What is varactor diode? [CO4 – L1]

A varactor diode is best explained as a variable capacitor. Think of the depletion region as a variable dielectric. The diode is placed in reverse bias. The dielectric is “adjusted” by reverse bias voltage changes.

• Junction capacitance is present in all reverse biased diodes because of the depletion region.

• Junction capacitance is optimized in a varactor diode and is used for high frequencies and switching applications.

• Varactor diodes are often used for electronic tuning applications in FM radios and televisions.

PART B

1. Explain the operation of zener diode and how it is used as a voltage egulator. [CO4 – L2 - Nov/Dec 2015] [12]

Zener diode

A Zener diode is a type of diode that permits current not only in the forward direction like a normal diode, but also in the reverse direction if the voltage is larger than the breakdown voltage known as "Zener knee voltage" or "Zener voltage". The device was named after Clarence Zener, who discovered this electrical property.

Diode symbol

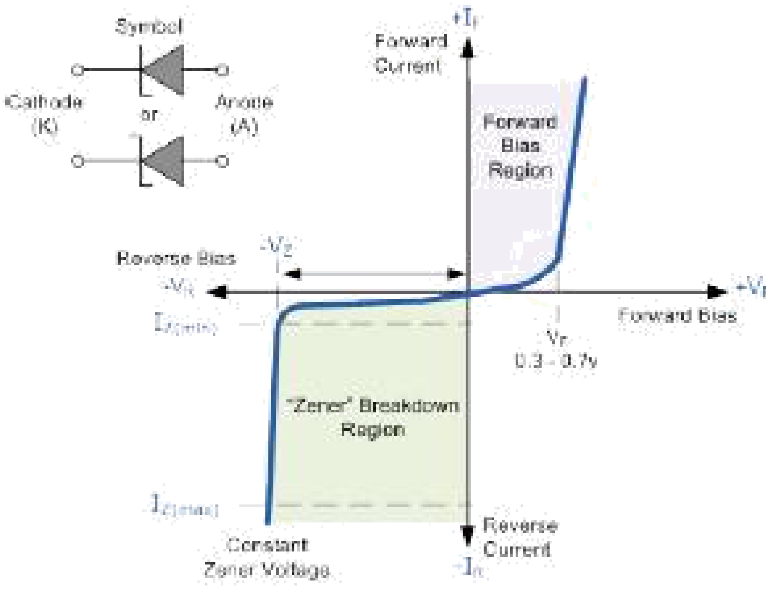
However, the Zener Diode or "Breakdown Diode" as they are sometimes called, are basically the same as the standard PN junction diode but are specially designed to have a low pre-determined Reverse Breakdown Voltage that takes advantage of this high reverse voltage. The point at which a zener diode breaks down or conducts is called the "Zener Voltage" (V_z).

The Zener diode is like a general-purpose signal diode consisting of a silicon PN junction. When biased in the forward direction it behaves just like a normal signal diode passing the rated current, but when a reverse voltage is applied to it the reverse saturation current remains fairly constant over a wide range of voltages. The reverse voltage increases until the diodes breakdown voltage VB is reached at which point a process called Avalanche Breakdown occurs in the depletion layer and the current flowing through the zener diode increases dramatically to the maximum circuit value (which is usually limited by a series resistor). This breakdown voltage point is called the "zener voltage" for zener diodes.

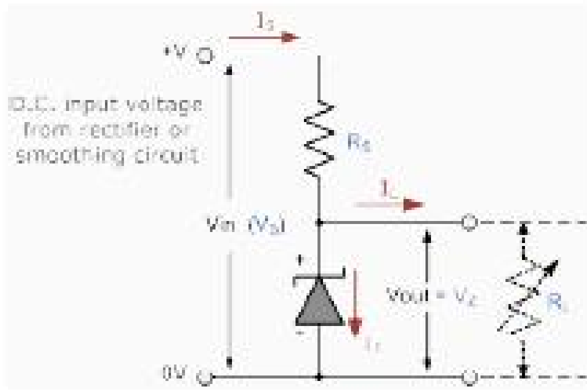
The point at which current flows can be very accurately controlled (to less than 1% tolerance) in the doping stage of the diodes construction giving the diode a specific *zener breakdown voltage*, (V_z) ranging from a few volts up to a few hundred volts. This zener breakdown voltage on the I-V curve is almost a vertical straight line.

Zener diode characteristics

The Zener Diode is used in its "reverse bias" or reverse breakdown mode, i.e. the diodes anode connects to the negative supply. From the I-V characteristics curve above, we can see that the zener diode has a region in its reverse bias characteristics of almost a constant negative voltage regardless of the value of the current flowing through the diode and remains nearly constant even with large changes in current as long as the zener diodes current remains between the breakdown current $I_{Z(min)}$ and the maximum current rating $I_{Z(max)}$.



The Zener Diode Regulator



Zener Diodes can be used to produce a stabilised voltage output with low ripple under varying load current conditions. By passing a small current through the diode from a voltage source, via a suitable current limiting resistor (RS), the zener diode will conduct sufficient current to maintain a voltage drop of Vout. We remember from the previous tutorials that the DC output voltage from the half or full-wave rectifiers contains ripple superimposed onto the DC voltage and that as the load value changes so to does the average output voltage. By connecting a simple zener stabiliser circuit as shown below across the output of the rectifier, a more stable output voltage can be produced**.**

3. Explain the operation of Schottky Barrier diode. [CO4 – L2 - May/June 2013] [8]

Schottky Barrier (Hot-Carrier) Diodes:

In recent years, there has been increasing interest in a two-terminal device referred to as a Schottky-barrier, surface-barrier, or hot-carrier diode. Its areas of application were first limited to the very high frequency range due to its quick response time (especially important at high frequencies) and a lower noise figure (a quantity of real importance in high-frequency applications). In recent years, however, it is appearing more and more in low-voltage/high-current power supplies and ac-to-dc converters.

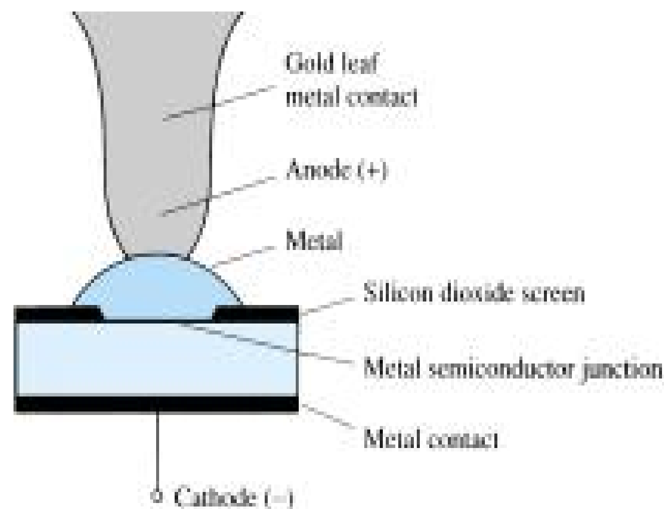


Fig 1. Passivated schottky barrier diode

Its construction is quite different from the conventional p-n junction in that a metalsemiconductor junction is created such as shown in Fig.1. The semiconductor is normally n-type silicon (although p-type silicon is sometimes used), while a host of different metals, such as molybdenum, platinum, chrome, or tungsten, are used. Different construction techniques will result in a different set of characteristics for the device, such as increased frequency range, lower forward bias, and so on. Priorities do not permit an examination of each technique here, but information will usually be provided by the manufacturer. In general, however, Schottky diode construction results in a more uniform junction region and a high level of ruggedness.

In both materials, the electron is the majority carrier. In the metal, the level of minority carriers (holes) is insignificant. When the materials are joined, the electrons in the n-type silicon semiconductor material immediately flow into the adjoining metal, establishing a heavy flow of majority carriers. Since the injected carriers have a very

high kinetic energy level compared to the electrons of the metal, they are commonly called —hot carriers.‖

The additional carriers in the metal establish a —negative wall‖ in the metal at the boundary between the two materials. The net result is a —surface barrier‖ between the two materials, preventing any further current. That is, any electrons (negatively charged) in the silicon material face a carrier-free region and a —negative wall‖ at the surface of the metal.

The application of a forward bias as shown in the first quadrant of Fig. 2 will reduce the strength of the negative barrier through the attraction of the applied positive potential for electrons from this region. The result is a return to the heavy flow of electrons across the boundary, the magnitude of which is controlled by the level of the applied bias potential. The barrier at the junction for a Schottky diode is less than that of the p-n junction device in both the forward- and reverse-bias regions. The result is therefore a higher current at the same applied bias in the forward- and reverse-bias regions. This is a desirable effect in the forward-bias region but highly undesirable in the reverse-bias region.

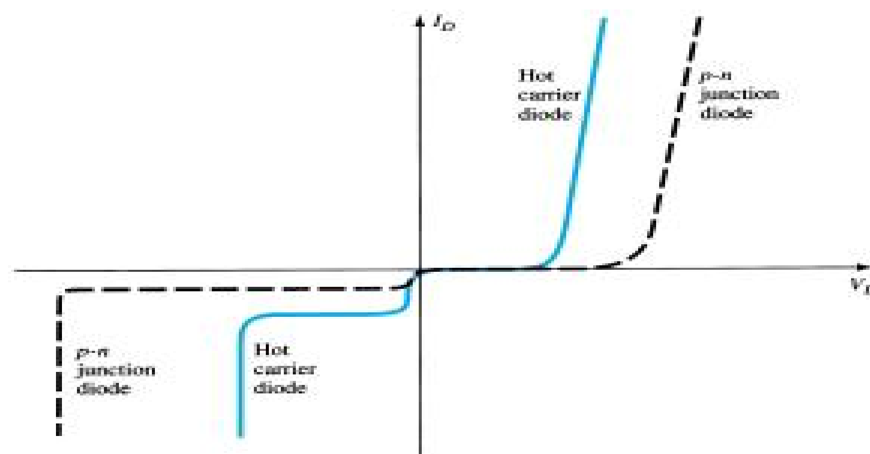


Fig 2. Comparison of characteristics of Hot carrier and pn diode

Applications

In radar systems,

Schottky TTL logicfor computers,

mixers and detectors in communication equipment,

instrumentation and analog-to-digital converters.

4. With neat diagram give the working principle of LASER diode [CO4 – L2 - May/June 2014] [8]

Laser diode:

A laser diode, or LD, is an electrically pumped semiconductor laser in which the active medium is formed by a p-n junction of a semiconductor diode similar to that found in a light-emitting diode.The laser diode is the most common type of laser produced. Laser diodes have a very wide range of uses that include, but are not limited to, fiber optic communications, barcode readers, laser pointers, CD/DVD/Blu-ray reading, laser printing, scanning and increasingly directional lighting sources.

A laser diode is electrically a P-i-n diode. The active region of the laser diode is in the intrinsic

(I) region, and the carriers, electrons and holes, are pumped into it from the N and P regions respectively. While initial diode laser research was conducted on simple P-N diodes, all modern lasers use the double-heterostructure implementation, where the carriers and the photons are confined in order to maximize their chances for recombination and light generation. Unlike a regular diode used in electronics, the goal for a laser diode is that all carriers recombine in the I region, and produce light. Thus, laser diodes are fabricated using direct bandgap semiconductors. The laser diode epitaxial structure is grown using one of the crystal growth techniques, usually starting from an N doped substrate, and growing the I doped active layer, followed by the P

doped cladding, and a contact layer. The active layer most often consists of quantum wells, which provide lower threshold current and higher efficiency.

Laser diodes form a subset of the larger classification of semiconductor *p*-*n* junction diodes. Forward electrical bias across the laser diode causes the two species of charge carrier – holes and electrons – to be "injected" from opposite sides of the *p*-*n* junction into the depletion region. Holes are injected from the *p*-doped, and electrons from the *n*-doped, semiconductor. (A depletion region, devoid of any charge carriers, forms as a result of the difference in electrical potential between *n*- and *p*-type semiconductors wherever they are in physical contact.) Due to the use of charge injection in powering most diode lasers, this class of lasers is sometimes termed "injection lasers," or "injection laser diode" (ILD). As diode lasers are semiconductor devices, they may also be classified as semiconductor lasers. Either designation distinguishes diode lasers from solid-state lasers.

When an electron and a hole are present in the same region, they may recombine or "annihilate" with the result being spontaneous emission — i.e., the electron may re-occupy the energy state of the hole, emitting a photon with energy equal to the difference between the electron and hole states involved. (In a conventional semiconductor junction diode, the energy released from the recombination of electrons and holes is carried away as phonons, i.e., lattice vibrations, rather than as photons.) Spontaneous emission gives the laser diode below lasing threshold similar properties to an LED. Spontaneous emission is necessary to initiate laser oscillation, but it is one among several sources of inefficiency once the laser is oscillating.

The difference between the photon-emitting semiconductor laser and conventional phonon-emitting (non-light-emitting) semiconductor junction diodes lies in the use of a different type of semiconductor, one whose physical and atomic structure confers the possibility for photon emission. These photon-emitting semiconductors are the so-

called "direct bandgap" semiconductors. The properties of silicon and germanium, which are single-element semiconductors, have bandgaps that do not align in the way needed to allow photon emission and are not considered "direct." Other materials, the so-called compound semiconductors, have virtually identical crystalline structures as silicon or germanium but use alternating arrangements of two different atomic species in a checkerboard-like pattern to break the symmetry. The transition between the materials in the alternating pattern creates the critical "direct bandgap" property. Gallium arsenide, indium phosphide, gallium antimonide, and gallium nitride are all examples of compound semiconductor materials that can be used to create junction diodes that emit light.

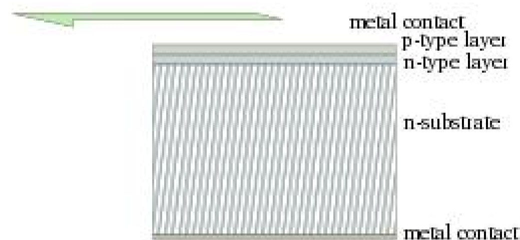


Diagram of a simple laser diode, such as shown above; not to scale

In the absence of stimulated emission (e.g., lasing) conditions, electrons and holes may coexist in proximity to one another, without recombining, for a certain time, termed the "upper-state lifetime" or "recombination time" (about a nanosecond for typical diode laser materials), before they recombine. Then a nearby photon with energy equal to the recombination energy can cause recombination by stimulated emission. This generates another photon of the same frequency, travelling in the same direction, with the same polarization and phase as the first photon. This means that stimulated emission causes

gain in an optical wave (of the correct wavelength) in the injection region, and the gain increases as the number of electrons and holes injected across the junction increases. The spontaneous and stimulated emission processes are vastly more efficient in direct bandgap semiconductors than in indirect bandgap semiconductors; therefore silicon is not a common material for laser diodes.

As in other lasers, the gain region is surrounded with an optical cavity to form a laser. In the simplest form of laser diode, an optical waveguide is made on that crystal surface, such that the light is confined to a relatively narrow line. The two ends of the crystal are cleaved to form perfectly smooth, parallel edges, forming a Fabry–Pérot resonator. Photons emitted into a mode of the waveguide will travel along the waveguide and be reflected several times from each end face before they are emitted. As a light wave passes through the cavity, it is amplified by stimulated emission, but light is also lost due to absorption and by incomplete reflection from the end facets. Finally, if there is more amplification than loss, the diode begins to "lase".Some important properties of laser diodes are determined by the geometry of the optical cavity. Generally, in the vertical direction, the light is contained in a very thin layer, and the structure supports only a single optical mode in the direction perpendicular to the layers. In the transverse direction, if the waveguide is wide compared to the wavelength of light, then the waveguide can support multiple transverse optical modes, and the laser is known as "multi-mode". These transversely multi-mode lasers are adequate in cases where one needs a very large amount of power, but not a small diffraction-limited beam; for example in printing, activating chemicals, or pumping other types of lasers.

In applications where a small focused beam is needed, the waveguide must be made narrow, on the order of the optical wavelength. This way, only a single transverse mode is supported and one ends up with a diffraction-limited beam. Such single spatial mode

devices are used for optical storage, laser pointers, and fiber optics. Note that these lasers may still support multiple longitudinal modes, and thus can lase at multiple wavelengths simultaneously.

The wavelength emitted is a function of the band-gap of the semiconductor and the modes of the optical cavity. In general, the maximum gain will occur for photons with energy slightly above the band-gap energy, and the modes nearest the gain peak will lase most strongly. If the diode is driven strongly enough, additional *side modes* may also lase. Some laser diodes, such as most visible lasers, operate at a single wavelength, but that wavelength is unstable and changes due to fluctuations in current or temperature.

Due to diffraction, the beam diverges (expands) rapidly after leaving the chip, typically at 30 degrees vertically by 10 degrees laterally. A lens must be used in order to form a collimated beam like that produced by a laser pointer. If a circular beam is required, cylindrical lenses and other optics are used. For single spatial mode lasers, using symmetrical lenses, the collimated beam ends up being elliptical in shape, due to the difference in the vertical and lateral divergences. This is easily observable with a red laser pointer.

5. Explain the operation of varactor diode [CO4 – L2 - May/June 2014] [8]

Varactor Diode:

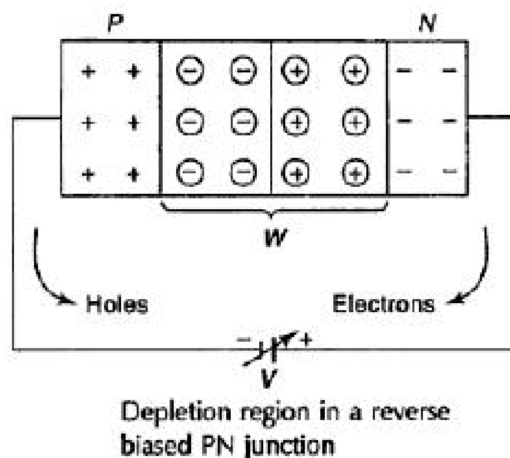
A varactor diode is best explained as a variable capacitor. Think of the depletion region as a variable dielectric. The diode is placed in reverse bias. The dielectric is ―adjusted‖ by reverse bias voltage changes.

- Junction capacitance is present in all reverse biased diodes because of the depletion region.

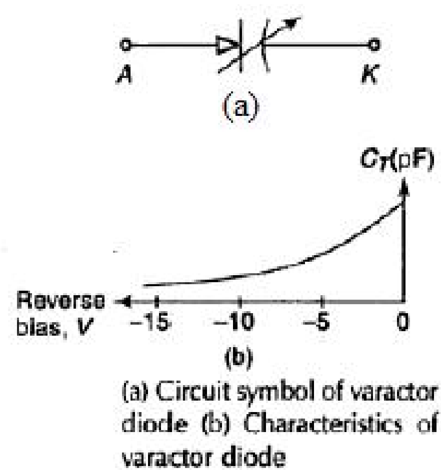
• Junction capacitance is optimized in a varactor diode and is used for high frequencies and switching applications.

• Varactor diodes are often used for electronic tuning applications in FM radios and televisions.

- They are also called voltage-variable capacitance diodes.
- A Junction diode which acts as a variable capacitor under changing reverse bias is known as VARACTOR DIODE
- A varactor diode is specially constructed to have high resistance under reverse bias. Capacitance for varactor diode are Pico farad. (10-12) range



Depletion region in a reverse biased PN junction



(a) Circuit symbol of varactor diode (b) Characteristics of varactor diode

CT = ЄA / Wd

CT =Total Capacitance of the junction

Є = Permittivity of the semiconductor material

A = Cross sectional area of the junction WD= Width of the depletion layer

Curve between Reverse bias voltage Vr across varactor diode and total junction capacitance Ct and Ct can be changed by changing Vr.

6. with neat diagram explain about Tunnel diode, Mention its advantages and Disadvantages [CO4 – L2 - Nov/Dec 2015] [10]

Tunnel diode (Esaki Diode)

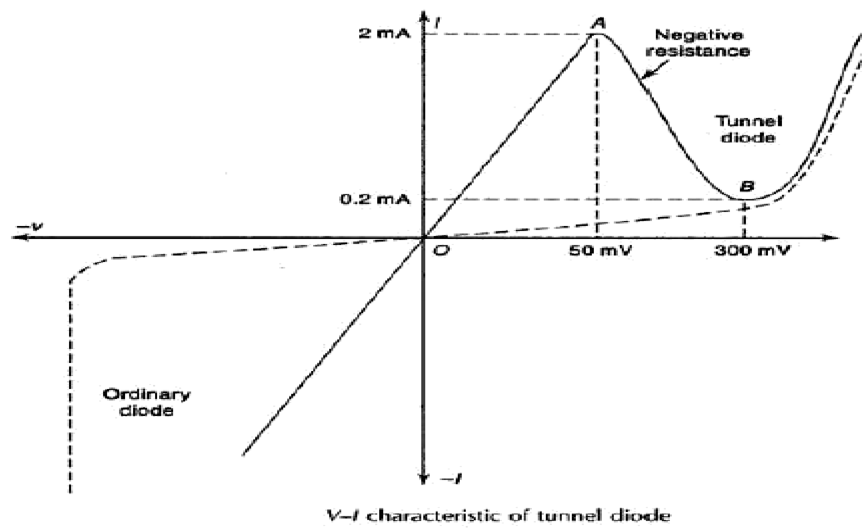
- It was introduced by Leo Esaki in 1958.
- Heavily-doped p-n junction

Impurity concentration is 1 part in 10^3 as compared to 1 part in 10^8 in p-n junction diode

- Width of the depletion layer is very small (about 100 A).
- It is generally made up of Ge and GaAs.
- It shows tunneling phenomenon.
- Circuit symbol of tunnel diode is :

Tunnelling Effect

- Classically, carrier must have energy at least equal to potential-barrier height to cross the junction .
- But according to Quantum mechanics there is finite probability that it can penetrate through the barrier for a thin width.
- This phenomenon is called tunneling and hence the Esaki Diode is known as Tunnel Diode.



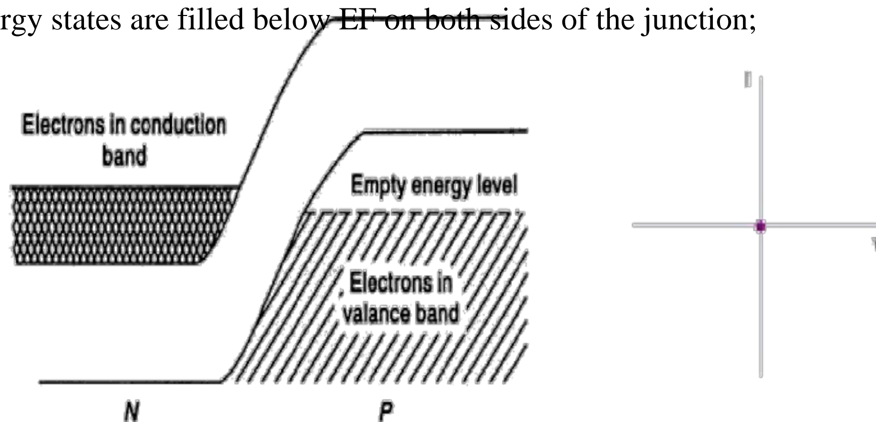
V–I characteristic of tunnel diode

ENERGY BAND DIAGRAM

Energy-band diagram of pn junction in thermal equilibrium in which both the n and p region are degenerately doped.

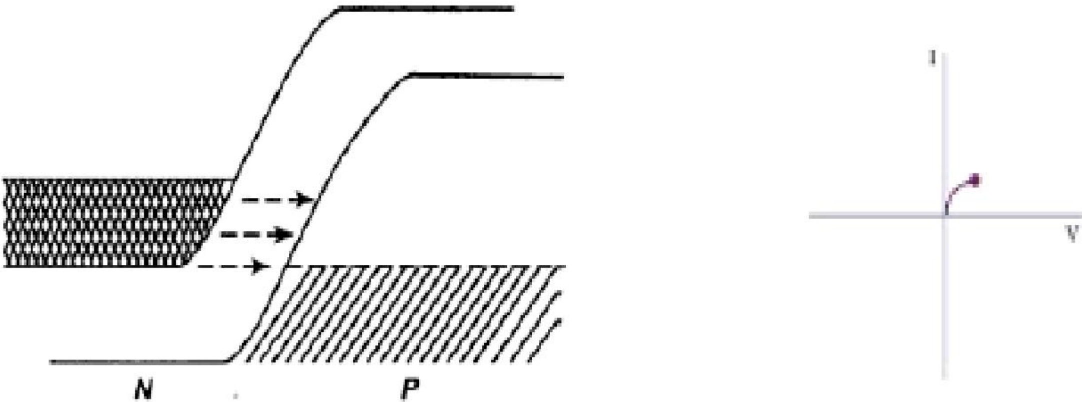
AT ZERO BIAS:Simplified energy-band diagram and I-V characteristics of the tunnel diode at zero bias.

- Zero current on the I-V diagram;
- All energy states are filled below EF on both sides of the junction;



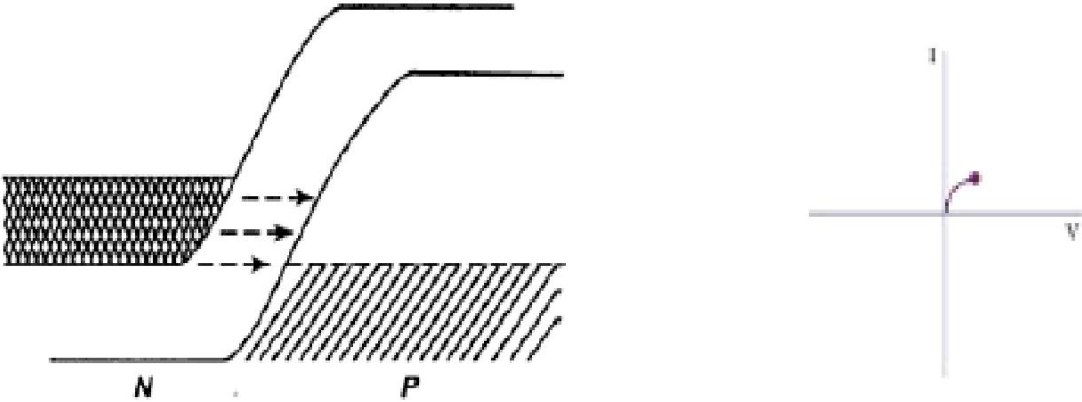
AT SMALL FORWARD VOLTAGE

Simplified energy-band diagram and I-V characteristics of the tunnel diode at a slight forward bias



AT SMALL FORWARD VOLTAGE

Simplified energy-band diagram and I-V characteristics of the tunnel diode at a slight forward bias



Electrons in the conduction band of the n region are directly opposite to the empty states in the valence band of the p region.

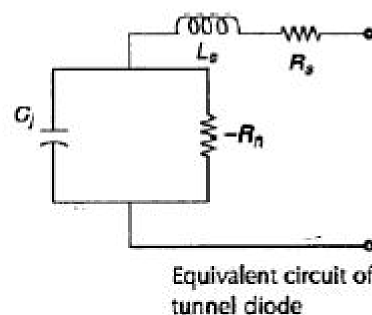
So a finite probability that some electrons tunnel directly into the empty states resulting in forward-bias tunneling current.

AT MAXIMUM TUNNELING CURENT

Simplified energy-band diagraam and I-V characteristics of the tunnel diode at a forward bias producing maximum tunneling current.

- The maximum number of electrons in the n region are opposite to the maximum number of empty states in the p region.
- Hence tunneling current is maximum.

TUNNEL DIODE EQUIVALENT CIRCUIT



Equivalent circuit of tunnel diode

• This is the equivalent circuit of tunnel diode when biased in negative resistance region.

• At higher frequencies the series R and L can be ignored.

• Hence equivalent circuit can be reduced to parallel combination of junction capacitance and negative resistance.

Applications

- As logic memory storage device
- As microwave oscillator
- In relaxation oscillator circuit
- As an amplifier
- As an ultra-high speed switch

Advantages

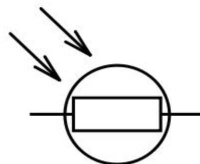
- Low noise
- Ease of operation
- High speed
- Low power

Disadvantages

- Voltage range over which it can be operated is 1 V less.
- Being a two terminal device there is no isolation between the input and output circuit.

7. Explain the operating Principle of LDR. [CO4 – L2 - May/June 2015] [8]

LDR:



A photoresistor or light-dependent resistor (LDR) or photocell is a resistor whose resistance decreases with increasing incident light intensity; in other words, it exhibits photoconductivity.A photoresistor is made of a high resistance semiconductor. If light

falling on the device is of high enough frequency, photons absorbed by the semiconductor give bound electrons enough energy to jump into the conduction band. The resulting free electron (and its hole partner) conduct electricity, thereby lowering resistance.A photoelectric device can be either intrinsic or extrinsic. An intrinsic semiconductor has its own charge carriers and is not an efficient semiconductor, for example, silicon. In intrinsic devices the only available electrons are in the valence band, and hence the photon must have enough energy to excite the electron across the entire bandgap. Extrinsic devices have impurities, also called dopants, added whose ground state energy is closer to the conduction band; since the electrons do not have as far to jump, lower energy photons (that is, longer wavelengths and lower frequencies) are sufficient to trigger the device. If a sample of silicon has some of its atoms replaced by phosphorus atoms (impurities), there will be extra electrons available for conduction. This is an example of an extrinsic semiconductor. There are many types of photoresistors, with different specifications and models. Photoresistors can be coated with or packaged in different materials that vary the resistance, depending on the use for each LDR.

Applications

Photoresistors come in many types. Inexpensive cadmium sulphide cells can be found in many consumer items such as camera light meters, street lights, clock radios, alarm devices, night lights, outdoor clocks, solar street lamps and solar road studs, etc.They are also used in some dynamic compressors together with a small incandescent lamp or light-emitting diode to control gain reduction.The use of CdS and CdSe photoresistors is severely restricted in Europe due to the RoHS ban on cadmium.Lead sulphide (PbS) and indium antimonide (InSb) LDRs (light-dependent resistor) are used for the mid-infrared spectral region. Ge:Cu photoconductors are among the best far-

infrared detectors available, and are used for infrared astronomy and infrared spectroscopy.

Unit - V

Power Devices and Display Devices

Part - A

1. What is intrinsic stand- off ratio of an UJT? [CO5 – L1 - May/June 2014]

If a voltage V_{BB} is applied between the bases with emitter open the circuit will behave as a potential divider. Thus the voltage V_{BB} will be divided across R_{B1} and R_{B2}

Voltage across resistance R_{B1},

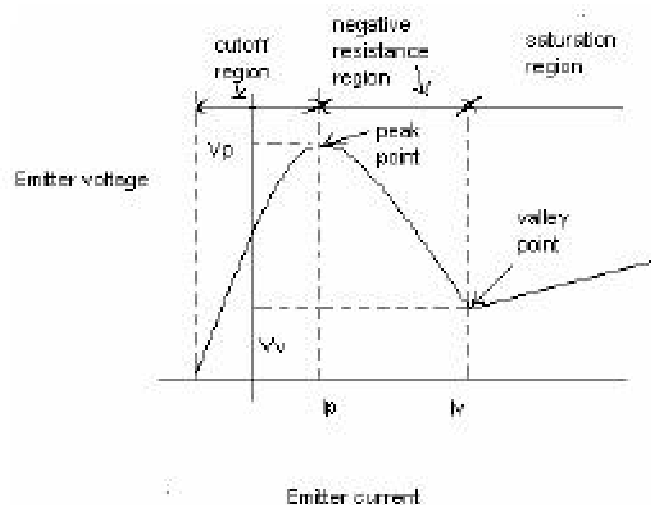
The resistance ratio $\eta = R_{B1} / R_{BB}$ is known as intrinsic stand -off ratio.

$$V_1 = \frac{R_{B1}}{R_{B1} + R_{B2}} * V_{BB}$$

$$= \frac{R_{B1}}{R_{BB}} * V_{BB}$$

$$= \eta * V_{BB}$$

2. Give the V-I characteristics of UJT. [CO5 – L1 - May/June 2015]

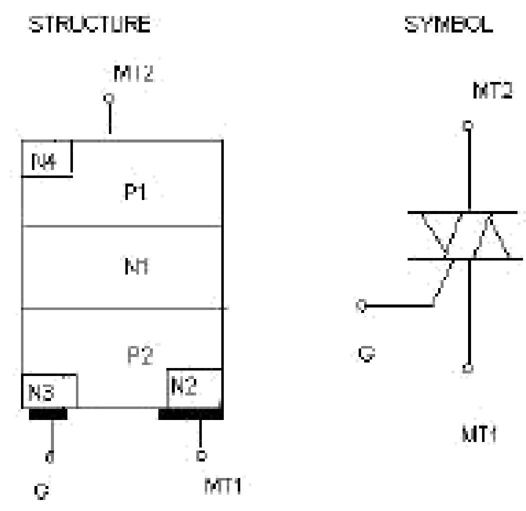


3. Mention the applications of UJT. [CO5 – L2]

1. It is used in timing circuits
2. It is used in switching circuits
3. It is used in phase control circuits
4. It can be used as trigger device for SCR and triac.
5. It is used in saw tooth generator.
6. It is used for pulse generation

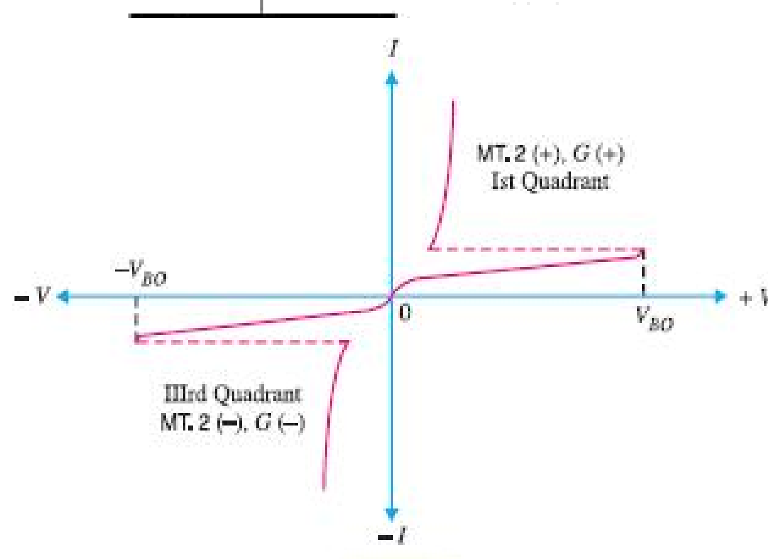
4. What is a TRIAC? Give the symbol and structure of TRIAC. [CO5 – L1 - May/June 2015]

TRIAC is a three terminal bidirectional semiconductor switching device. It can conduct in both the directions for any desired period. In operation it is equivalent to two SCR's connected in antiparallel.



MT2

5. Draw the V-I characteristics for TRIAC. [CO5 – L1]



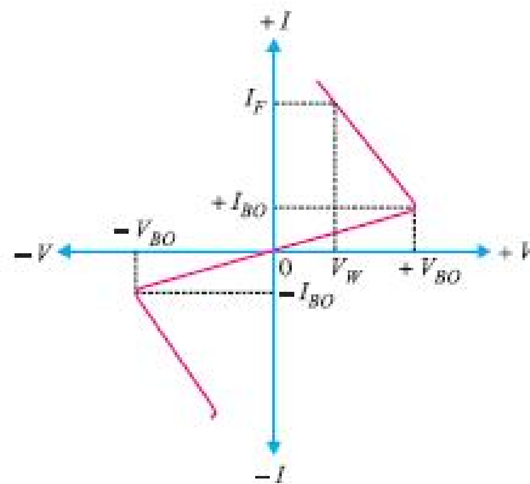
6. Give the application of TRIAC. [CO5 – L2 - May/June 2015]

1. Heater control
2. Motor speed control
3. Phase control
4. Static switches

7. What is a DIAC? Give the basic construction and symbol of DIAC. [CO5 – L1]

DIAC is a two terminal bidirectional semiconductor switching device. . It can conduct in either direction depending upon the polarity of the voltage applied across its main terminals. In operation DIAC is equivalent to two 4 layer diodes connected in antiparallel.

8. Draw the V-I curve for DIAC [CO5 – L1 - Nov/Dec 2013]



9. Give some applications of DIAC. [CO5 – L2 - May/June 2013]

1. To trigger TRIAC
2. Motor speed control
3. Heat control
4. Light dimmer circuits

10. Why SCR cannot be used as a bidirectional switch. [CO5 – L2 - May/June 2015]

SCR can do conduction only when anode is positive with respect to cathode with proper gate current. Therefore, SCR operates only in one direction and cannot be used as bidirectional switch.

11. How turning on of SCR is done? [CO5 – L2]

1. By increasing the voltage across SCR above forward break over voltage.
2. By applying a small positive voltage at gate.
3. By rapidly increasing the anode to cathode voltage.
4. By irradiating SCR with light.

12. How turning off of SCR is done? [CO5 – L2]

1. By reversing the polarity of anode to cathode voltage.
2. By reducing the current through the SCR below holding current.
3. By interrupting anode current by means of momentarily series or parallel switching

13. Define holding current in a SCR. [CO5 – L1]

Holding current is defined as the minimum value of anode current to keep the SCR ON.

14. List the advantages of SCR. [CO5 – L1]

1. SCR can handle and control large currents.
2. Its switching speed is very high
3. It has no moving parts, therefore it gives noiseless operation.
4. Its operating efficiency is high.

15. List the application of SCR. [CO5 – L2 - May/June 2013]

1. It can be used as a speed controller in DC and AC motors.
2. It can be used as an inverter.

3. It can be used as a converter
4. It is used in battery chargers.
5. It is used for phase control and heater control.
6. It is used in light dimming control circuits

16. Compare SCR with TRIAC [CO5 – L2 - May/June 2015]

SCR	TRIAC
I. unidirectional current	I. bidirectional current
2. triggered by positive pulse at gate	2. triggered by pulse of positive or negative al pate
3. last turn of! lime	3.. longer turn off time
4.large current ratings	4. lower current ratings

17. Differentiate BJT and UJT. [CO5 – L1 - May/June 2015]

BJT	UJT
. It has two PN junctions	I. It has only one PN junctions
. three terminals present are emitter, base, ol lector	2. three terminals present are emitter, base 1.base 2
. basically a amplifying device	3. basically a switching device

18. State the principle of operation of an LED [CO5 – L1 - Nov/Dec 2014]

When a free electron from the higher energy level gets recombined with the hole, it gives the light output. Here in case of LEDs, the supply of higher level electrons is provided by the battery connection.

19. Give the advantages of LED [CO5 – L1 - May/June 2015]

They are small in size.

Light in weight. Mechanically rugged. Low operating temperature.

Switch on time is very small. Available in different colours.

They have longer life compared to larrps

Linearity is better.

Compatible with ICs.

Low cost.

20. State some disadvantages of LED [CO5 – L2 - May/June 2014]

Output power gets affected by the temperature radiation.

Quantum efficiency is low.

Gets damaged due to over -voltage and over-current.

21. List the applications of LED [CO5 – L2 - Nov/Dec 2015]

They are used in various types of displays.

They are used as source in opto-couplers.

Used in infrared remote controls.

Used as indicator lamps.

Used as indicators in measuring devices.

22. Give some advantages and disadvantages for LCD of LCD [CO5 – L1]

Low power is required

Good contrast

Low cost

Disadvantages of LCD

Speed of operation is slow

LCD occupy a large area

LCD life span is quite small, when used on d.c. Therefore, they are used with a.c. suppliers.

23. Give applications of LCD [CO5 – L2 - May/June 2013]

Used as numerical counters for counting production items.

Analog quantities can also be displayed as a number on a suitable device. (e.g.) Digital multimeter.

Used for solid state video displays.

Used for image sensing circuits.

Used for image sensing circuits.

Used for numerical display in pocket calculators.

24. Compare LEDs and LCDs. [CO5 – L2 - May/June 2015]

LEDs	LCDs
1. More power is required. 2. Fastest displays 3. More life. 4. LED is light source. 5. More temperature range. 6. Mounting is easy	1. Less power is required. 2. Slowest displays. 3. Less life. 4. LCD is not light source. It is a light reflector. 5. Less temperature range 6. Mounting is difficult.

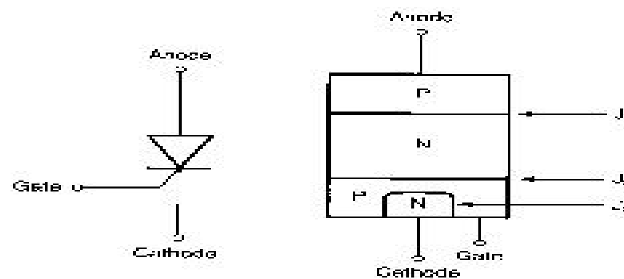
25. Give some notes on CCD. [CO5 – L1]

A charge-coupled device (CCD) is a device for the movement of electrical charge, usually from within the device to an area where the charge can be manipulated, for example conversion into a digital value. This is achieved by "shifting" the signals

between stages within the device one at a time. CCDs move charge between capacitive *bins* in the device, with the shift allowing for the transfer of charge between bins. The CCD is a major piece of technology in digital imaging. In a CCD image sensor, pixels are represented by p-doped MOS capacitors.

PART B

1. Explain the construction, operation, V-I characteristics and application of SCR and explain its two transistor model. [CO5 – L2 - May/June 2015] [16]



Silicon Controlled Rectifier (SCR):

Three terminals

anode - P-layer

cathode - N-layer (opposite end)

gate - P-layer near the cathode

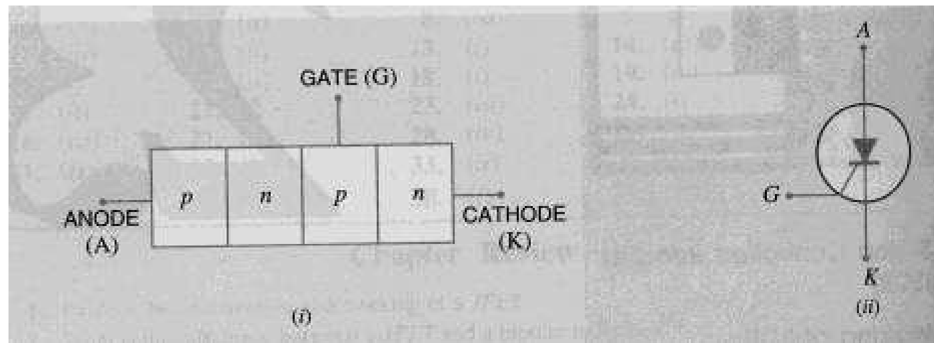
Three junctions - four layers

Connect power such that the anode is positive with respect to the cathode - no current will flow

A silicon controlled rectifier is a semiconductor device that acts as a true electronic switch. It can change alternating current and at the same time can control the amount of power fed to the load. SCR combines the features of a rectifier and a transistor.

Construction

When a pn junction is added to a junction transistor the resulting three pn junction device is called a SCR. ordinary rectifier (pn) and a junction transistor (npn) combined in one unit to form pnpn device. three terminals are taken :

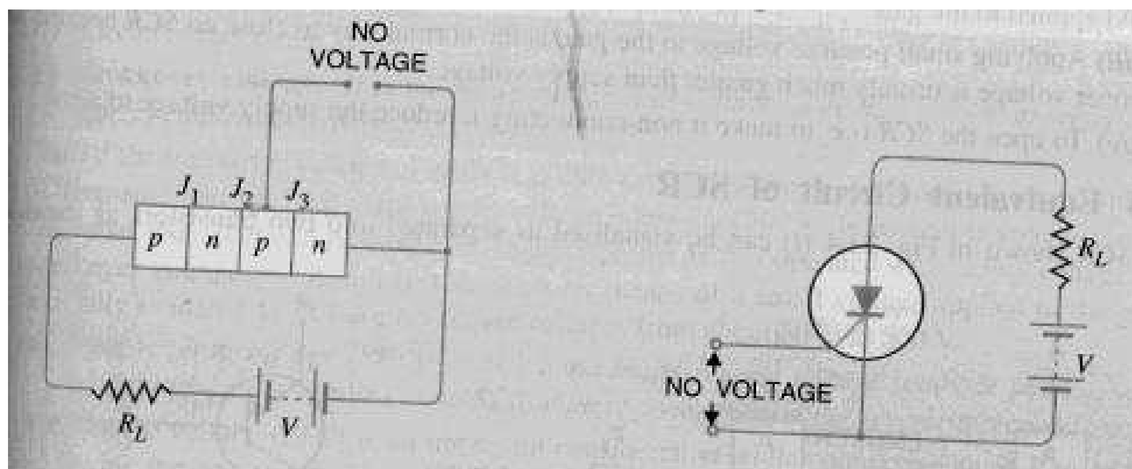


one from the outer p- type material called anode a second from the outer n- type material called cathode K and the third from the base of transistor called Gate. GSCR is a solid state equivalent of thyratron. the gate anode and cathode of SCR correspond to the grid plate and cathode of thyratron SCR is called thyristor.

Working Principle

Load is connected in series with anode the anode is always kept at positive potential w.r.t cathode.

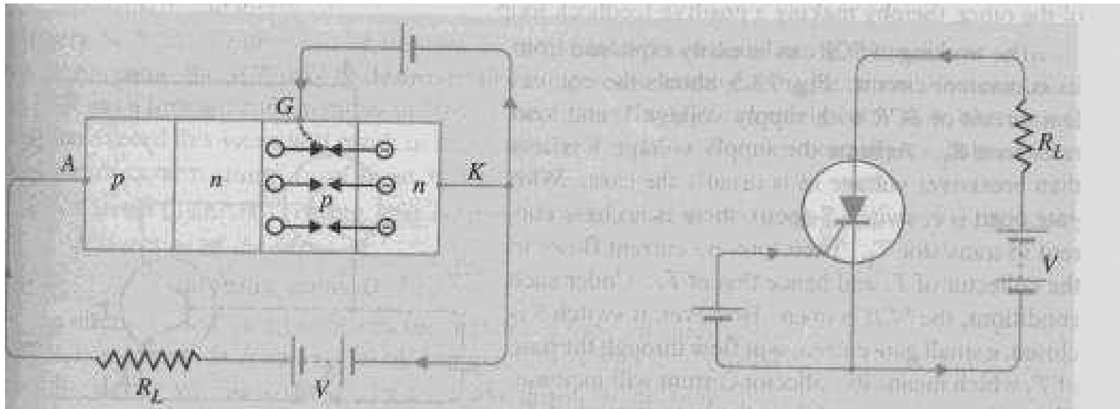
When Gate Is Open



No voltage applied to the gate, j2 is reverse biased while j1 and j3 are FB . J1 and J3 is just in npn transistor with base open .no current flows through the load RL and SCR is cut off. If the applied voltage is gradually increased a stage is reached when RB junction

J2 breakdown .the SCR now conducts heavily and is said to be ON state. the applied voltage at which SCR conducts heavily without gate voltage is called Break over Voltage.

When Gate Is Positive W.R.T Cathode.



SCR can be made to conduct heavily at smaller applied voltage by applying small positive potential to the gate.J3 is FB and J2 is RB the electron from n type material start moving across J3 towards left holes from p type toward right. electrons from j3 are attracted across junction J2 and gate current starts flowing. as soon as gate current flows anode current increases. the increased anode current in turn makes more electrons available at J2 breakdown and SCR starts conducting heavily. the gate loses all control if the gate voltage is removed anode current does not decrease at all. The only way to stop conduction is to reduce the applied voltage to zero.

Breakover Voltage

It is the minimum forward voltage gate being open at which SCR starts conducting heavily i.e turned on.

Peak Reverse Voltage(PRV)

It is the maximum reverse voltage applied to an SCR without conducting in the reverse direction.

Holding Current

It is the maximum anode current gate being open at which SCR is turned off from on conditions.

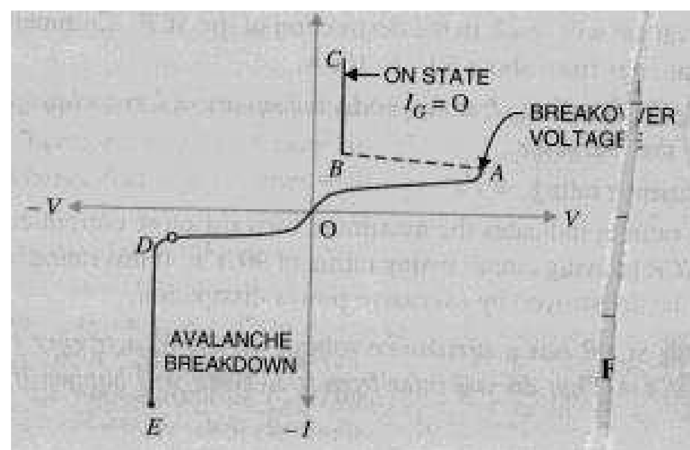
Forward Current Rating

It is the maximum anode current that an SCR is capable of passing without destruction

Circuit Fusing Rating

It is the product of of square of forward surge current and the time of duration of the surge.

VI Characteristics of SCR:



Forward Characteristics:

When anode is +ve w.r.t cathode the curve between V & I is called Forward characteristics. OABC is the forward characteristics of the SCR at Ig =0. if the supplied

voltage is increased from zero point A is reached .SCR starts conducting voltage across SCR suddenly drops (dotted curve AB) most of supply voltage appears across RL

Reverse Characteristics:

When anode is –ve w.r.t.cathode the curve b/w V&I is known as reverse characteristics reverse voltage come across SCR when it is operated with ac supply reverse voltage is increased anode current remains small avalanche breakdown occurs and SCR starts conducting heavily is known as reverse breakdown voltage

Application

SCR as a switch

SCR Half and Full wave rectifier

SCR as a static contactor

SCR for power control

SCR for speed control of d.c.shunt motor

Over light detector

2. Explain the construction , operation, equivalent circuit V-I characteristics and application of UJT [CO5 – L2 - May/June 2015] [16]

Uni Junction Transistor (UJT):

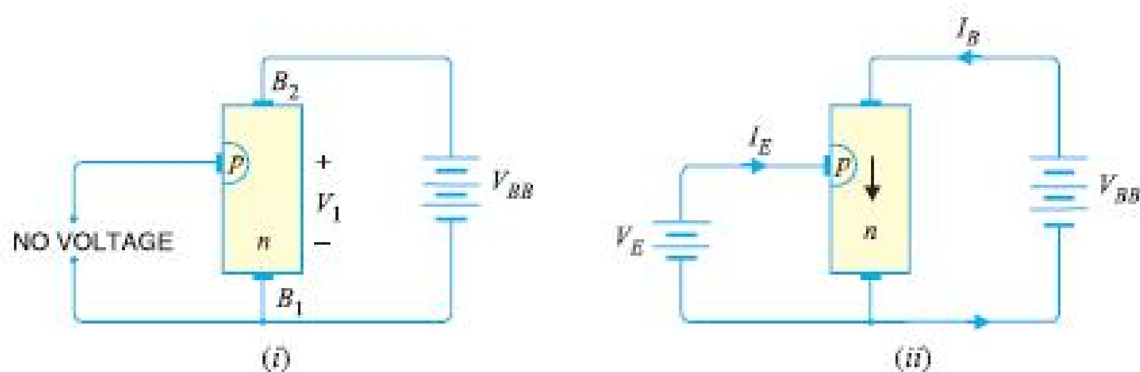
A uni junction transistor (UJT) is an electronic semiconductor device that has only one junction.

The UJT has three terminals: an emitter (E) and two bases (B1 and B2).

The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is open-circuit is called interbase resistance.

Since the device has one pn junction and three leads it is commonly called UJT.

Operation



The device has normally B2 is positive w.r.t B1.

(i) If voltage V_{BB} is applied between B2 and B1 with emitter open (fig. i) a voltage gradient is established along the n type bar. The voltage V1 between emitter and B1 establishes a reverse bias of pn junction and the emitter current is cut off. Small leakage current flows from B2 to emitter.

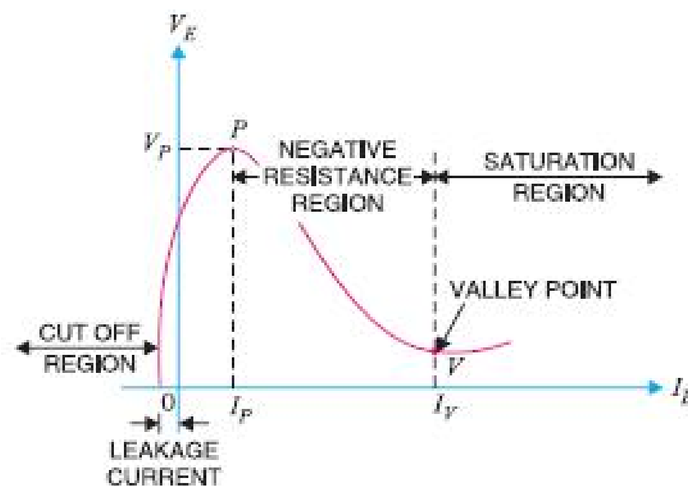
(ii)If a positive voltage is applied at E (fig. ii) the pn junction remains reverse biased as long as the input is less than V1. The voltage exceeds V1 the pn junction become forward biased. Here holes are injected from p type towards B1. The device is ON state.

(iii) If a negative pulse is applied to E, the pn junction is reverse biased and the emitter current is cut off. The device is OFF state.

Characteristics

Initially in the cut off region, as V_E increases from zero, slight leakage current flows from terminalB2 to the emitter.

Above a certain value of V_E forward I_E begins to flow, increasing until the peak voltage Vp and current Ip are reached at point P.



After the peak point P an attempt to increase V_E is followed by a sudden increase in emitter current I_E with a corresponding decrease in V_E. This is a negative resistance portion of the curve because in I_E, V_E decreases.

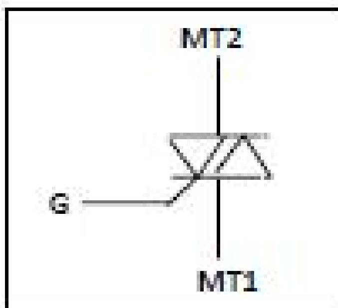
Applications

In switching circuits, Pulse generator and Saw-tooth generator.

3. Explain the construction , operation, equivalent circuit V-I characteristics and application of TRIAC [CO5 – L2 - May/June 2014] [16]

TRIAC:

Triacs are three terminal devices that are used to switch large a.c. currents with a small trigger signal. Triacs are commonly used in dimmer switches, motor speed control circuits and equipment that automatically controls mains powered equipment including remote control. The triac has many advantages over a relay, which could also be used to control mains equipment; the triac is cheap, it has no moving parts making it reliable and it operates very quickly.



The three terminals on a triac are called Main Terminal 1 (MT1), Main Terminal 2(MT2) and Gate (G). To turn on the triac there needs to be a small current IGT flowing through the gate, this current will only flow when the voltage between G and MT1 is at least

VGT. The signal that turns on the triac is called the trigger signal. Once the triac is turned on it will stay on even if there is no gate current until the current flowing between MT2 and MT1 fall below the hold current IH.

Operation

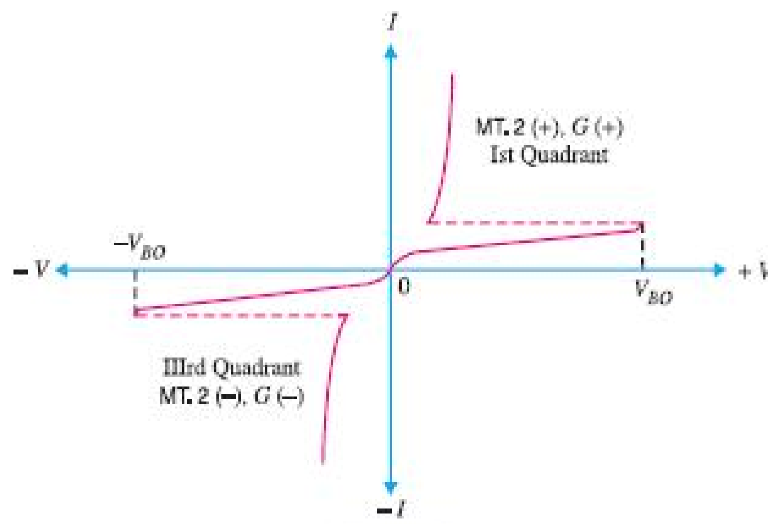
With switch S open, there will be no gate current and the triac is cut off. Even with no current the triac can be turned on provided the supply voltage becomes equal to the breakover voltage.

When switch S is closed, the gate current starts flowing in the gate circuit. Breakover voltage of triac can be varied by making proper currnt flow. Triac starts to conduct wheather MT2 is positive or negative w.r.t MT1.

If terminal MT2 is positive w.r.t MT1 the triac is on and the conventional current will flow from MT2 to MT1.

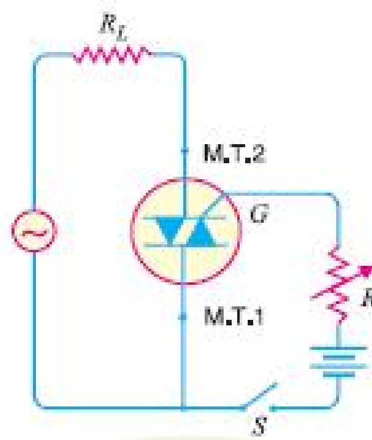
If terminal MT2 is negative w.r.t MT1 the triac is again turned on and the conventional current will flow from MT1 to MT2.

Characteristics:



The V-I curve for triac in the Ist and IIIrd quadrants are essentially identical to SCR in the Ist quadrant.

The triac can be operated with either positive or negative gate control voltage but in normal operation usually the gate voltage is positive in quadrant I and negative in quadrant III.



The supply voltage at which the triac is ON depends upon gate current. The greater gate current and smaller supply voltage at which triac is turned on. This permits to use

triac to control a,c. power in a load from zero to full power in a smooth and continuous manner with no loss in the controlling device.

4. Explain the construction, operation, equivalent circuit V-I characteristics and application of DIAC[CO5 – L2 - May/June 2014] [16]

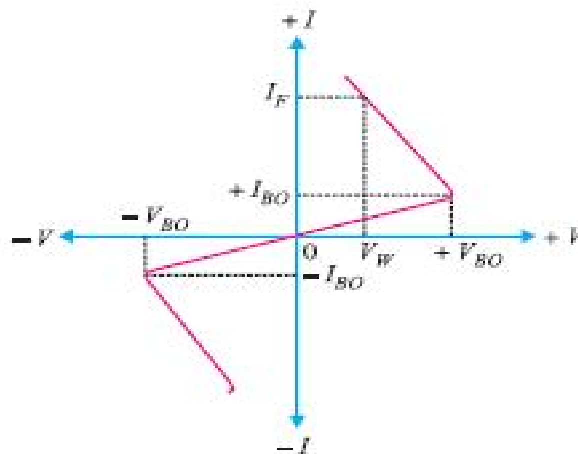
DIAC (Diode A.C. switch):

A Diac is two terminal , three layer bi directional device which can be switched from its off state for either polarity of applied voltage.

Operation

When a positive or negative voltage is applied across the terminals of Diac only a small leakage current Ibo will flow through the device as the applied voltage is increased , the leakage current will continue to flow until the voltage reaches breakover voltage Vbo at this point avalanche breakdown of the reverse biased junction occurs and the device exhibits negative resistance i.e current through the device increases with the decreasing values of applied voltage the voltage across the device then drops to breakback voltage Vw.

V- I Characteristics Of A DIAC:



For applied positive voltage less than + Vbo and Negative voltage less than -Vbo , a small leakage current flows thrugh the device. Under such conditions the diac blocks flow of current and behaves as an open circuit. the voltage +Vbo and -Vbo are the breakdown voltages and usually have range of 30 to 50 volts.

When the positive or negative applied voltage is equal to or greater than tha breakdown voltage Diac begins to conduct and voltage drop across it becomes a few volts conduction then continues until the device current drops below its holding current breakover voltage and holding current values are identical for the forward and reverse regions of operation.

Applications

Diacs are used for triggering of triacs in adjustable phase control of a c mains power. Applications are light dimming heat control universal motor speed control.

5. Explain about VMOS [CO5 – L2 - Nov/Dec 2015] [8]

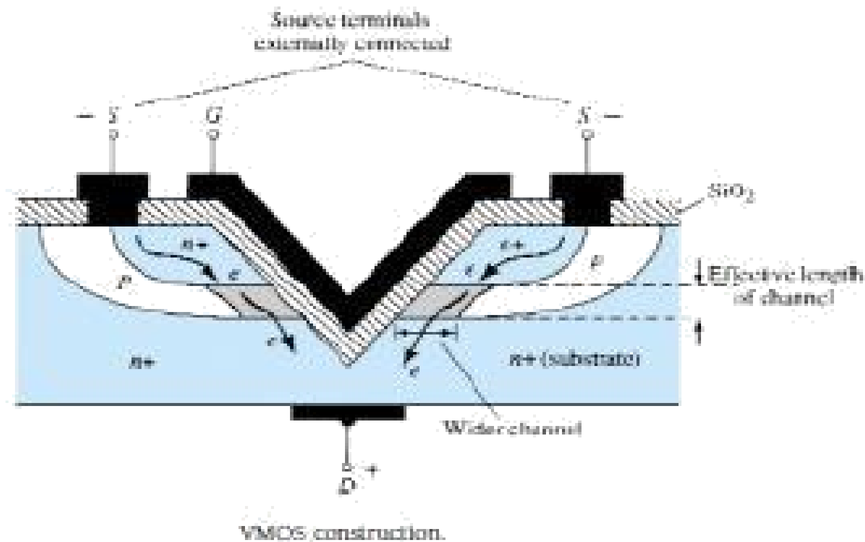
VMOS

One of the disadvantages of the typical MOSFET is the reduced power-handling levels (typically, less than 1 W) compared to BJT transistors. This shortfall for a device with so many positive characteristics can be softened by changing the construction mode from one of a planar nature to one with a vertical structure as shown in Fig.

All the elements of the planar MOSFET are present in the vertical metal-oxide-silicon FET (VMOS)—the metallic surface connection to the terminals of the device—the SiO2 layer between the gate and the p-type region between the drain and source for the growth of the induced n-channel (enhancement- mode operation). The term vertical is due primarily to the fact that the channel is now formed in the vertical direction rather than the horizontal direction for the planar device.

However, the channel of Fig. also has the appearance of a ―V‖ cut in the semiconductor base, which often stands out as a characteristic for mental memorization of the name of the device. The construction of Fig is somewhat simplistic in nature, leaving out some of the transition levels of doping, but it does permit a description of the most important facets of its operation.

The application of a positive voltage to the drain and a negative voltage to the source with the gate at 0 V or some typical positive ―on‖ level as shown in Fig. will result in the induced n-channel in the narrow p-type region of the device. The length of the channel is now defined by the vertical height of the p-region, which can be made significantly less than that of a channel using planar construction. On a horizontal plane the length of the channel is limited to 1 to 2 µm.



VMOS construction.

Diffusion layers can be controlled to small fractions of a micrometer. Since decreasing channel lengths result in reduced resistance levels, the power dissipation level of the device (power lost in the form of heat) at operating current levels will be reduced. In addition, the contact area between the channel and the no region is greatly increased by the vertical mode construction, contributing to a further decrease in the resistance level and an increased area for current between the doping layers.

There is also the existence of two conduction paths between drain and source, as shown in Fig., to further contribute to a higher current rating. The net result is a device with drain currents that can reach the ampere levels with power levels exceeding 10 W.

Compared with commercially available planar MOSFETs, VMOS FETs have reduced channel resistance levels and higher current and power ratings.

VMOS FETs have a positive temperature coefficient that will combat the possibility of thermal runaway.

The reduced charge storage levels result in faster switching times for VMOS construction compared to those for conventional planar construction.

In fact, VMOS devices typically have switching times less than one-half that encountered for the typical BJT transistor.

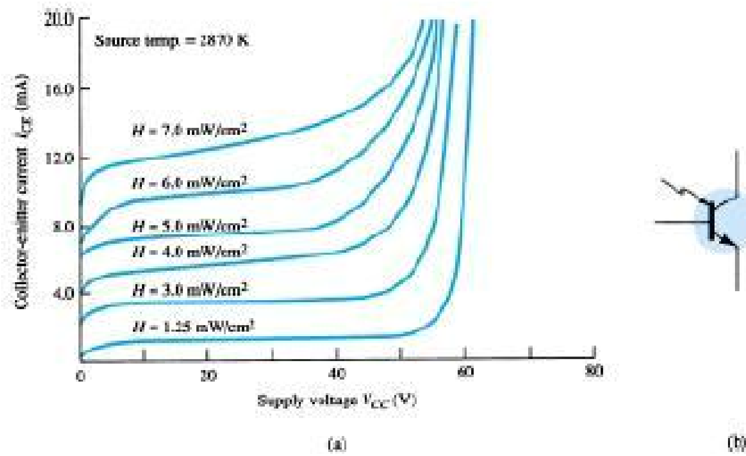
6. Explain the operation of Photo transistor [CO5 – L2 - Nov/Dec 2015] [8]

Photo Transistors:

Phototransistor, has a photosensitive collector–base p-n junction. The current induced by photoelectric effects is the base current of the transistor. If we assign the notation I for the photoinduced base current, the resulting collector current, on an approximate basis, is

$$I_C = h_{fe} I_A$$

A representative set of characteristics for a phototransistor is provided in Fig. with the symbolic representation of the device. Note the similarities between these curves and those of a typical bipolar transistor. As expected, an increase in light intensity corresponds with an increase in collector current. To develop a greater degree of familiarity with the light-intensity unit of measurement, milliwatts per square centimeter, a curve of base current versus flux density appears in Fig.. Note the exponential



increase in base current with increasing flux density. In the same figure, a sketch of the phototransistor is provided with the terminal identification and the angular alignment.

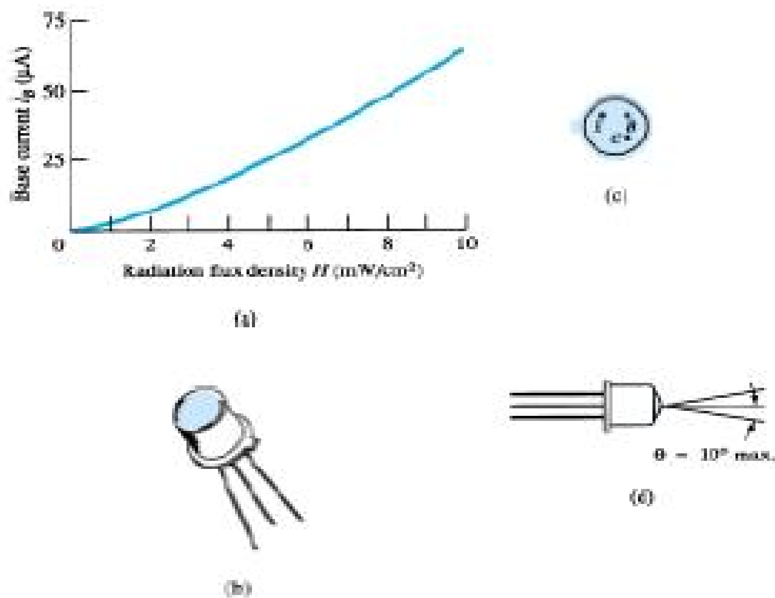
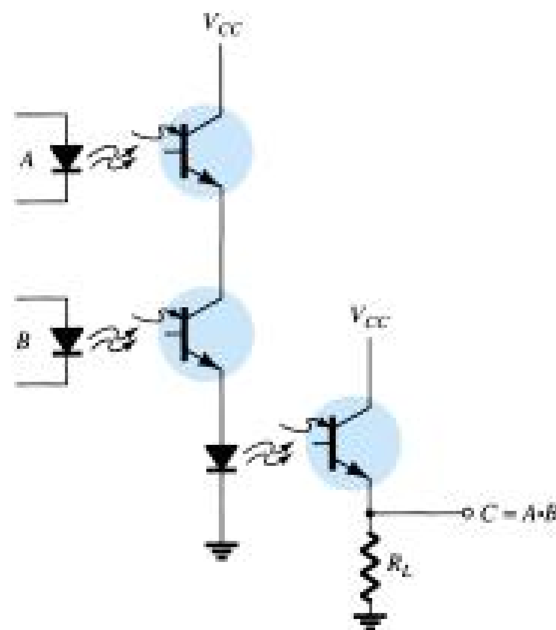


Photo Transistor (a) collector characteristics (b) symbol

Phototransistor (a) base current vs flux density (b) Device

(c) Terminal identification (d) angular alignment

A high-isolation AND gate is shown in Fig using three phototransistors and three LEDs (light-emitting diodes). The LEDs are semiconductor devices that emit light at an intensity
determined by the forward current through the device. The terminology high isolation simply refers to the lack of an electrical connection between the input and output circuits.



High isolation AND gate employing phototransistor and LED

Applications

Some of the areas of application for the phototransistor include punch-card readers, computer logic circuitry, lighting control (highways, etc.), level indication, relays, and counting systems.

7. With neat diagram explain the operation of Solar cell. [CO5 – L2 - Nov/Dec 2015] [8].

Solar Cells:

In recent years, there has been increasing interest in the solar cell as an alternative source of energy. When we consider that the power density received from the sun at sea level is about 100 mW/cm^2 (1 kW/m2), it is certainly an energy source that requires further research and development to maximize the conversion efficiency from solar to electrical energy.

The basic construction of a silicon p-n junction solar cell appears in Fig. 1. As shown in the top view, every effort is made to ensure that the surface area perpendicular to the sun is a maximum. Also, note that the metallic conductor connected to the p-type material and the thickness of the p-type material are such that they ensure that a maximum number of photons of light energy will reach the junction. A photon of light energy in this region may collide with a valence electron and impart to it sufficient energy to leave the parent atom. The result is a generation of free electrons and holes. This phenomenon will occur on each side of the junction.

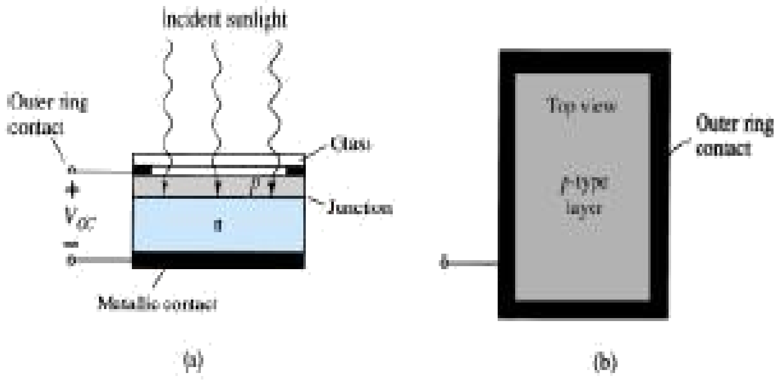


Fig 1. (a) cross section; (b) top view

In the p-type material, the newly generated electrons are minority carriers and will move rather freely across the junction as explained for the basic p-n junction with no applied bias. A similar discussion is true for the holes generated in the n-type material. The result is an increase in the minority-carrier flow, which is opposite in direction to the conventional forward current of a p-n junction. This increase in reverse current is shown in Fig. 2. Since V= 0 anywhere on the vertical axis and represents a short-circuit condition, the current at this intersection is called the short-circuit current and is represented by the notation I_{SC}.

Under open-circuit conditions (id = 0), the photovoltaic voltage V_{OC} will result. This is a logarithmic function of the illumination, as shown in Fig. 3. V_{OC} is the terminal voltage of a battery under no-load (open-circuit) conditions. Note, however, in the same figure that the short-circuit current is a linear function of the illumination. That is, it will double for the same increase in illumination (f_{C1} and $2f_{C1}$ in Fig. 3) while the change in V_{OC} is less for this region. The major increase in V_{OC} occurs for lower-level increases

in illumination. Eventually, a further increase in illumination will have very little effect on V_{OC}, although I_{SC} will increase, causing the power capabilities to increase.

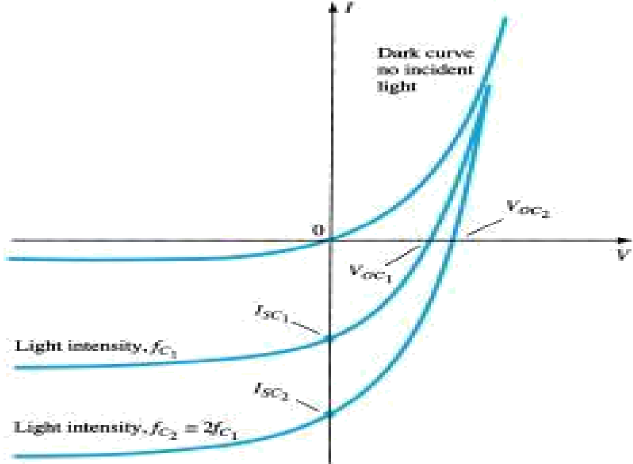


Fig 2. V-I curve for solar cell

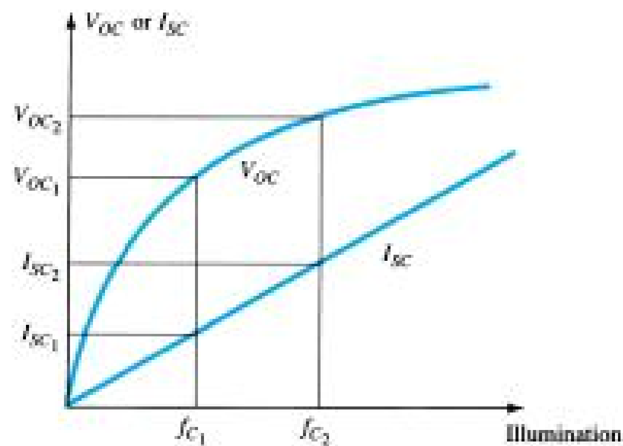


Fig 3. Voc and Isc versus illumination for solar cell

Selenium and silicon are the most widely used materials for solar cells, although gallium arsenide, indium arsenide, and cadmium sulfide, among others, are also used.

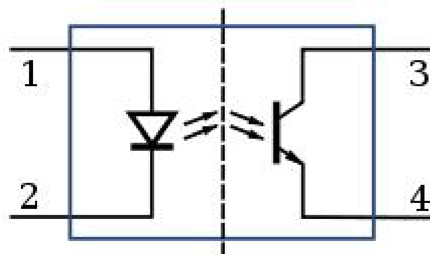
8. Explain the following (a) Optocoupler (b) CCD [CO5 – L2 - Nov/Dec 2014] [8]

Opto Coupler:

In electronics, an opto-isolator, also called an optocoupler, photocoupler, or optical isolator, is a component that transfers electrical signals between two isolated circuits by using light. Opto-isolators prevent high voltages from affecting the system receiving the signal. Commercially available opto-isolators withstand input-to-output voltages up to 10 kV and voltage transients with speeds up to 10 kV/ μs. A common type of opto-isolator consists of an LED and a phototransistor in the same package. Opto-isolators are usually used for transmission of digital (on/off) signals, but some techniques allow use with analog (proportional) signals.

An opto-isolator contains a source (emitter) of light, almost always a near infrared light-emitting diode (LED), that converts electrical input signal into light, a closed optical channel (also called dielectrical channel), and a photosensor, which detects incoming

light and either generates electric energy directly, or modulates electric current flowing from an external power supply.



The sensor can be a photoresistor, a photodiode, a phototransistor, a silicon-controlled rectifier (SCR) or a triac. Because LEDs can sense light in addition to emitting it, construction of symmetrical, bidirectional opto-isolators is possible. An optocoupled solid state relay contains a photodiode opto-isolator which drives a power switch, usually a complementary pair of MOSFETs. A slotted optical switch contains a source of light and a sensor, but its optical channel is open, allowing modulation of light by external objects obstructing the path of light or reflecting light into the sensor.

CCD:

A charge-coupled device (CCD) is a device for the movement of electrical charge, usually from within the device to an area where the charge can be manipulated, for example conversion into a digital value. This is achieved by "shifting" the signals between stages within the device one at a time. CCDs move charge between capacitive *bins* in the device, with the shift allowing for the transfer of charge between bins. The CCD is a major piece of technology in digital imaging. In a CCD image sensor, pixels are represented by p-doped MOS capacitors. These capacitors are biased above the threshold for inversion when image acquisition begins, allowing the conversion of incoming photons into electron charges at the semiconductor-oxide interface; the CCD is then used to read out these charges. Although CCDs are not the only technology to

allow for light detection, CCD image sensors are widely used in professional, medical, and scientific applications where high-quality image data is required. In applications with less exacting quality demands, such as consumer and professional digital cameras, active pixel sensors (CMOS) are generally used; the large quality advantage CCDs enjoyed early on has narrowed over time.

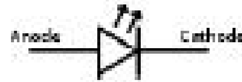
9. Explain the following(a) LED (b) LCD [CO5 – L2 - Nov/Dec 2015] [16]

Light Emitting Diode (LED):

A light-emitting diode (LED) is a semiconductor light source. LEDs are used as indicator lamps in many devices, and are increasingly used for lighting. Introduced as a practical electronic component in 1962, early LEDs emitted low-intensity red light, but modern versions are available across the visible, ultraviolet and infrared wavelengths, with very high brightness.

When a light-emitting diode is forward biased (switched on), electrons are able to recombine with electron holes within the device, releasing energy in the form of photons. This effect is called electroluminescence and the color of the light (corresponding to the energy of the photon) is determined by the energy gap of the semiconductor. An LED is often small in area (less than 1 mm2), and integrated optical components may be used to shape its radiation pattern.[3] LEDs present many advantages over incandescent light sources including lower energy consumption, longer lifetime, improved robustness, smaller size, faster switching, and greater durability and reliability. LEDs powerful enough for room lighting are relatively expensive and require more precise current and heat management than compact fluorescent lamp sources of comparable output.

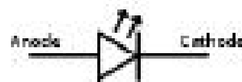
SYMBOL OF LED

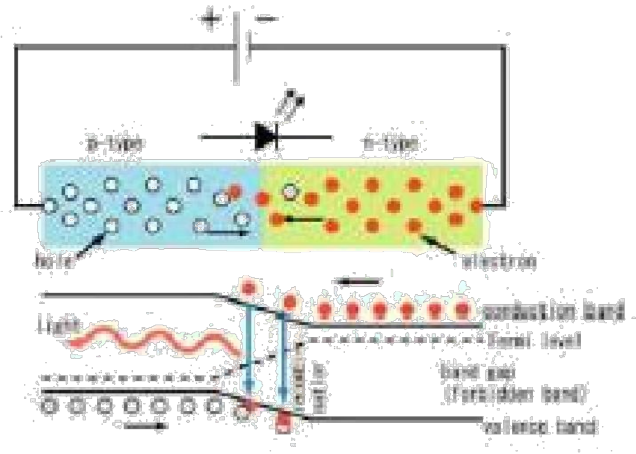


When a light-emitting diode is forward biased (switched on), electrons are able to recombine with electron holes within the device, releasing energy in the form of photons. This effect is called electroluminescence and the color of the light (corresponding to the energy of the photon) is determined by the energy gap of the semiconductor. An LED is often small in area (less than 1 mm2), and integrated optical components may be used to shape its radiation pattern.[3] LEDs present many advantages over incandescent light sources including lower energy consumption, longer lifetime, improved robustness, smaller size, faster switching, and greater durability and reliability. LEDs powerful enough for room lighting are relatively expensive and require more precise current and heat management than compact fluorescent lamp sources of comparable output.

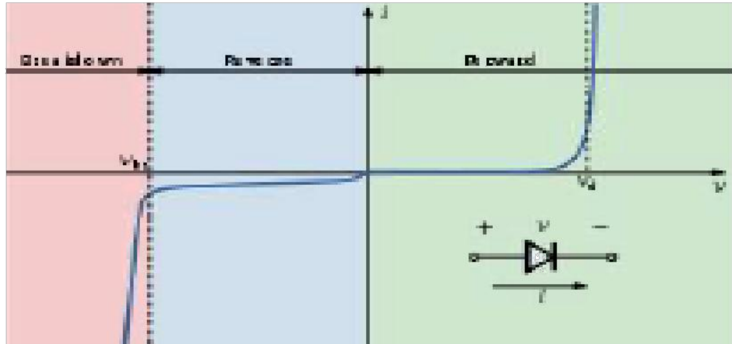
Light-emitting diodes are used in applications as diverse as replacements for aviation lighting, automotive lighting (particularly brake lamps, turn signals and indicators) as well as in traffic signals. The compact size, the possibility of narrow bandwidth, switching speed, and extreme reliability of LEDs has allowed new text and video displays and sensors to be developed, while their high switching rates are also useful in advanced communications technology. Infrared LEDs are also used in the remote control units of many commercial products including televisions, DVD players, and other domestic appliances.

SYMBOL OF LED





DIODE I-V CURVE



Liquid-Crystal Displays:

The liquid-crystal display (LCD) has the distinct advantage of having a lower power requirement than the LED. It is typically in the order of microwatts for the display, as compared to the same order of milliwatts for LEDs. It does, however, require an external or internal light source and is limited to a temperature range of about 0° to

60°C. Lifetime is an area of concern because LCDs can chemically degrade. The types receiving the major interest today are the field-effect and dynamic-scattering units.
A liquid crystal is a material (normally organic for LCDs) that will flow like a liquid but whose molecular structure has some properties normally associated with solids. For the light- scattering units, the greatest interest is in the nematic liquid crystal, having the crystal structure shown in Fig 1.

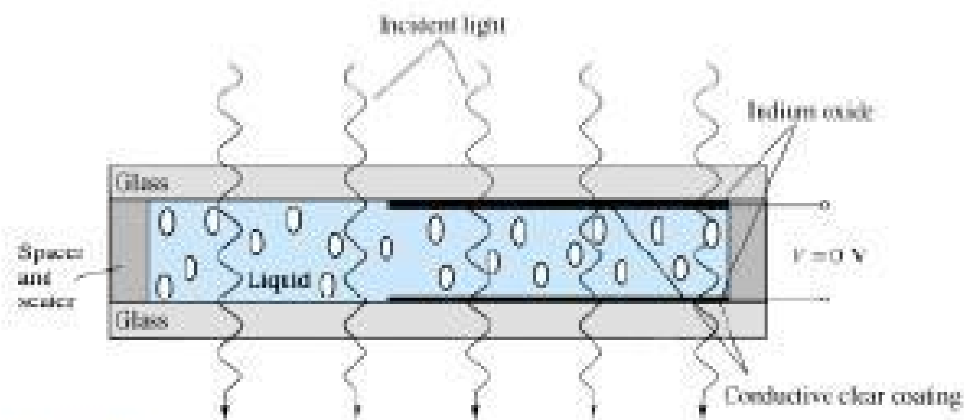


Figure 1 Nematic liquid crystal with no applied bias.

The individual molecules have a rod like appearance as shown in the figure. The indium oxide conducting surface is transparent, and under the condition shown in the figure, the incident light will simply pass through and the liquid-crystal structure will appear clear. If a voltage (for commercial units the threshold level is usually between 6 and 20 V) is applied across the conducting surfaces, as shown in Fig. 2, the molecular arrangement is disturbed, with the result that regions will be established with different indices of refraction.

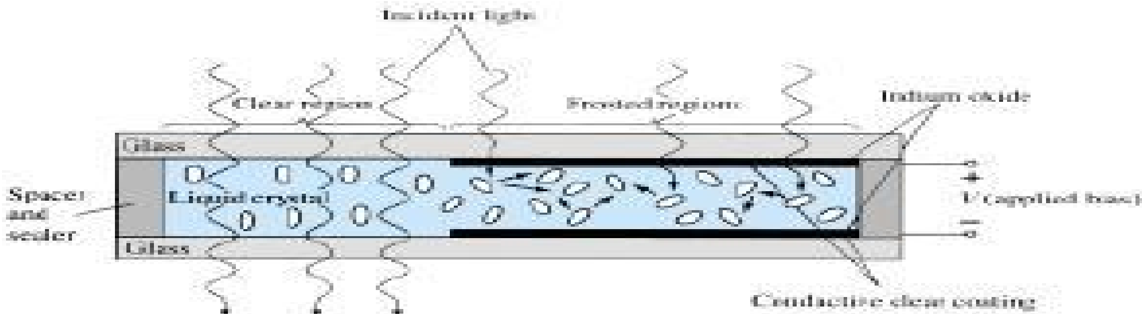


Figure 2 Nematic liquid crystal with applied bias.

A digit on an LCD display may have the segment appearance shown in Fig. 3. The black area is actually a clear conducting surface connected to the terminals below for external control. Two similar masks are placed on opposite sides of a sealed thick layer of liquid-crystal material. If the number 2 were required, the terminals 8, 7, 3, 4, and 5 would be energized, and only those regions would be frosted while the other areas would remain clear.

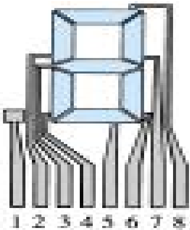
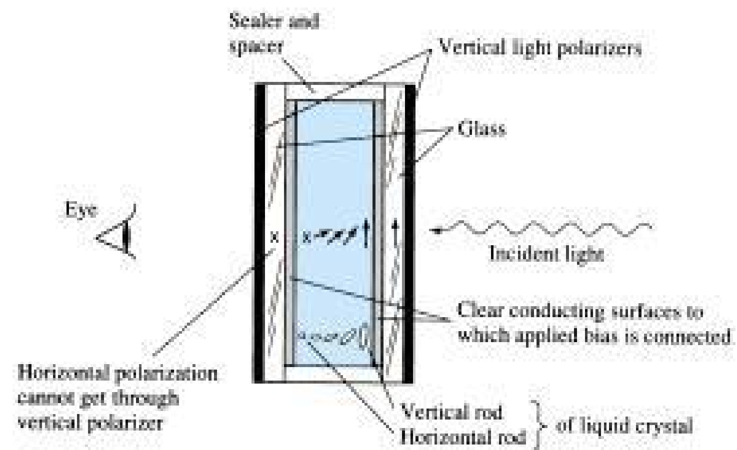


Fig 3. LCD 8 segment digit display

The field-effect or twisted nematic LCD has the same segment appearance and thin layer of encapsulated liquid crystal, but its mode of operation is very different. Similar to the dynamic-scattering LCD, the field-effect LCD can be operated in the reflective or transmissive mode with an internal source. The transmissive display appears in Fig. 4. The internal light source is on the right, and the viewer is on the left.



This figure is most noticeably different from Fig. 20.35 in that there is an addition of a light polarizer. Only the vertical component of the entering light on the right can pass through the vertical-light polarizer on the right.

The reflective-type field-effect LCD is shown in Fig. 5. In this case, the horizontally polarized light at the far left encounters a horizontally polarized filter and passes through to the reflector, where it

is reflected back into the liquid crystal, bent back to the other vertical polarization, and returned to the observer. If there is no applied voltage, there is a uniformly lit display. The application of a voltage results in a vertically incident light encountering a horizontally polarized filter at the left, which it will not be able to pass through and will be reflected.

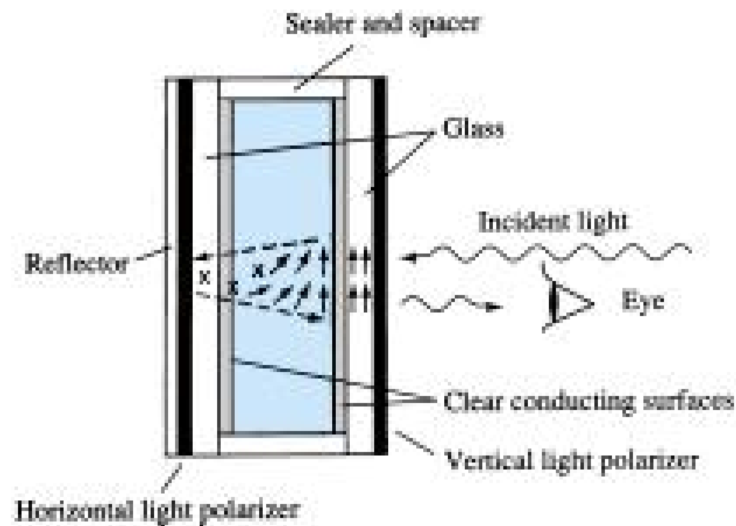


Fig 5. Reflective field effect LCD with no applied bias

Advantages of LCD

Low power is required

Good contrast

Low cost

Disadvantages of LCD

Speed of operation is slow

LCD occupy a large area

LCD life span is quite small, when used on d.c. Therefore, they are used with a.c. suppliers.

Applications of LCD

Used as numerical counters for counting production items.

- Analog quantities can also be displayed as a number on a suitable device. (e.g.) Digital multimeter.

- Used for solid state video displays.□
- Used for image sensing circuits.
- Used for numerical display in pocket calculators.